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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR DEVICES

IBM

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Silicon Dioxide
Hole Traps

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

These papers discuss electron trapping on sites related to H_2O, the subsequent interface states generated by the trapping, and the reduction of these traps by high temperature nitrogen annealing. Radiation induced neutral trapping centers are discussed in relation to electron or hole capital on them. A new electrically alterable memory device using a dual electron injector structure composed of silicon-rich silicon dioxide and silicon dioxide layers is described. Material characterization is

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the Fi-rich SiO_2 film, discussed using attenuated total reflectance, raman scattering, and optical absorption measurements. Detection of trap impurities, on Fi surfaces is studied using electron trapping character techniques.

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II. Summary of Work Performed Under This Contract

The rapid evolution of high density integrated circuits has required a careful examination and control of all the vital materials involved. The thin insulating layer (SiO_2) used for the MOSFETs is a crucial material that has required this work which is the focus of this contract. In addition, the background that has been developed concerning the injection of electronic current into this material from either silicon or from an external gate conductor has enabled us to significantly reduce the voltage required for the onset of current injection by using thin (100-250 Å) silicon rich layers near the electrodes. This has application for use in writing and erasing charge storage devices. The practical importance of this application has required a partial shift in emphasis as this project has progressed.

The initial statement of work to be performed on the contract is listed below.

1. Completion of the study of the oxidation of polycrystalline silicon including the investigation of means to reduce the asperities normally present on polycrystalline silicon.

2. Completion of the work on the effect of electron traps in the electrical breakdown of SiO_2. This will include measurements on the effect of field distortion deliberately introduced by trapping charge on impurity sites to learn more about the breakdown mechanism.

3. We have observed the importance of the post oxidation annealing procedure on electron trapping in normal dry SiO_2 as measured at 77°K and 300°K; however, the optimum annealing procedure is different for the two temperatures. We would like to gain an understanding of these effects by varying the gas ambient used and by using the photo I-V technique to determine the location of the traps.

4. Completion of our investigation of the exciton model as an explanation for the interface state generation at the Si-SiO_2 interface resulting from the application of non penetrating VUV radiation to the SiO_2 with negative gate bias.

5. Completion of studies of photo detrapping of electrons trapped on implanted As and P sites. This includes the understanding of the effect of optical interference on the results.

6. The results obtained to date have suggested new device possibilities for applications similar to those currently filled by MNOS and FAMOS devices. We plan to investigate these devices further to see if they warrant further development.

7. During the second year we will evaluate the properties of oxides made by the high pressure facility.

In the discussion that follows, the reference numbers will refer to the list of papers published contained in section III of this report.

The oxidation of polycrystalline silicon is discussed in papers 13 and 14 based on the work done by Irene, Tierney and Dong. The work proposed on electrical breakdown of SiO_2 has not been completed due to the increased emphasis on charge storage devices. The work on electrical trapping in SiO_2 has been reported in papers 8, 27, 28 and 29. In addition, we have been able to learn more about the microscopic details of the water related traps using attenuated total reflectance IR spectroscopy (30). It has been possible to make oxides recently with an extremely low electron trapping rate (28). This work has been done by Young, Irene, DiMaria, Massoud, Feigl, Lai, Calise, and Hartstein. We were fortunate to have Professor Frank Feigl with us for four months on leave from Lehigh University, who worked on the effect of water diffusion on the trapping characteristics (29).

The work on the exciton model has resulted in a publication (6) with the question still remaining concerning the validity of the proposed exciton model. This work was done by Weinberg, Young, DiMaria, and Rubloff. The electron trapping and detrapping characteristics of arsenic implanted SiO_2 layers has been studied by DeKeersmaecker and DiMaria (9,22) and has shown that implanted As results in a trap with a relatively large trapping cross section and that electrons trapped on this site can be detrapped using light.

As indicated earlier a major emphasis has been placed on studies relating to the use of thin Si-rich SiO_2 layers to enhance the injection of electronic current from electrodes (Si or Al) *into* SiO_2. This work has been "spearheaded" by DiMaria and has been done by DiMaria, Dong, Irene, Chou, Ghez, Hartstein, Kucza, Tsang, DeMeyer and Serrano as reported in 7, 15, 17, 19, 20, 21, 23, 24 and 26. This work has progressed rapidly and we are enthusiastic about the use of this technology in future products. The operation of these "charge injectors" depends on the two phase nature of Si rich SiO_2. The Si particles are small and densely packed. The electric field is enhanced by the presence of these particles and as a result electron current is injected at a reduced field. By using two layers (one near the control gate and one near the charge trapping storage layer or floating gate) it is possible to write and erase (charge and discharge the floating gate) using voltages that are compatible with those that can be produced by the selection circuits located on the same silicon chip. The presence of these silicon rich layers does not degrade the charge storage characteristics of the floating gate with the lower voltages applied for the reading process. Pleasant surprises have been the excellent reproducibility of the current voltage characteristics even when the materials are made in different furnaces, the large injection currents that can be obtained, and the observation that the presence of the silicon rich regions inhibits premature electrical breakdown effects. A major limitation at the present time results from electron trapping in the CVD-SiO_2 region located between the two Si-rich SiO_2 layers.

This limits the number of write-erase cycles to about 10^6 at the present time. We are trying to use our background in electron trapping to reduce the trapping rate and hence, increase the number of write-erase cycles.

We have not been able to study the transport properties of high pressure oxides since our high pressure oxidation facility is not yet functional. Some measurements have been made by Irene, Zeto and Dong on high pressure oxide samples supplied by Zeto of the Fort Monmouth, NJ Laboratory (12). Our work on the effects of radiation continues as reported by DiMaria, Ephrath and Young (5), and by Aitken (10,11). Work on hole trapping has been reported by DeKeersmaecker, DiMaria, and Aitken (16,31) and we have detected the presence of holes trapped in the "bulk" of the SiO_2 for the first time in this work. The later reference (31) shows that the neutral traps generated by radiation will trap holes as well as electrons.

As a result of problems arising in a manufacturing line, we have observed that Al inadvertantly left on the surface of a wafer can "float" up as the oxide is grown and be left at an interface between thermal SiO_2 and CVD SiO_2. The measurement techniques we have are capable of detecting an extremely small amount of Al at this interface. This is discussed in (25) based on the work of DiMaria, Reuter, Young, Pesavento and Calise. This work shows the crucial imprortance of the wafer cleaning process if an insulator-insulator interface is used.

MAJOR ACCOMPLISHMENTS

1. Charge injector structure developed to charge and discharge floating gate devices.

2. Water related trapping centers identified using attenuated total reflectance I.R. spectroscopy.

3. Techniques have been developed to make SiO_2 layers with an ultra low electron trapping rate.

4. Holes have been trapped in the bulk of the SiO_2 on neutral traps generated by radiation.

5. The effect of grain boundaries on the oxidation of polysilicon has been investigated.

6. Annealing of radiation-induced positive charge has been compared for Al and polysilicon gate electrodes.

7. Residual stress, etch rate, refractive index and density have been measured for SiO_2 prepared using high pressure oxygen.

8. Effect of low temperature ($\leq$ 300°C) water diffusion on the electron trapping in SiO_2 has been investigated.

III. Papers Published

1. "Silicon Oxidation Studies: Some Aspects of the Initial Oxidation Regime", E.A. Irene, *J. Electrochem. Soc.* 125, 1708, (1978).

2. "Some Observations of Defects in Amorphous SiO_2 Films", E.A. Irene, Proceedings of International Topical Conference on the Physics of SiO_2 and Its Interfaces, Ed. by S. Pantelides, Pergamon Inc., 1978.

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16. "Hole Trapping in the Bulk of SiO_2 Layers at Room Temperature", R.F. DeKeersmaecker and D.J. DiMaria, *J. Appl. Phys.* 51, 532 (1980).

17. "High Current Injection into SiO_2 from Si-Rich SiO_2 Films and Experimental Applications", D.J. DiMaria and D.W. Dong, *J. Appl. Phys.* 51, 2722 (1980).

18. "Charge Trapping Studies in SiO_2 Using High Current Injection from Si-rich SiO_2 FIlms", D.J. DiMaria, R. Ghez, and D.W. Dong, *J. Appl. Phys.* 51, 4830 (1980).

19. "Attenuated Total Reflectance Study of Silicon-Rich Silicon Dioxide Films", A. Hartstein, D.J. DiMaria, D.W. Dong and J.A. Kucza, *J. Appl. Phys.* 51, 3860 (1980). ***(Included in this report).***

20. "Observation of Amorphous Silicon Regions in Silicon-Rich Silicon Dioxide Films", A. Hartstein, J.C. Tsang, D.J. DiMaria, and D.W. Dong, *Appl. Phys. Lett.* 36, 836 (1980). ***(Included in this report)***

21. "Dual Electron Injector Structure", D.J. DiMaria and D.W. Dong, *Appl. Phys. Lett.* 37, 61 (1980). ***(Included in this report)***

22. "Electron Trapping and Detrapping Characteristics of Arsenic-Implanted SiO_2 Layers", R.F. DeKeersmaecker and D.J. DiMaria, in Insulating Films on Semiconductors 1979, Eds. G.G. Roberts and M.J. Morant (The Institute of Physics, Bristol and London, 1980), p. 40.

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25. "Detection of Impurities on Silicon Surfaces", D.J. DiMaria, W. Reuter, D.R. Young, F.L. Pesavento, and J.A. Calise, *submitted to J. Appl. Phys.*. ***(Included in this report)***.

26. "Electrically-Alterable Read-Only-Memory Using Si-Rich SiO_2 Injectors and a Floating Polycrystalline Silicon Storage Layer", D.J. DiMaria, K.M. DeMeyer, C.M. Serrano, and D.W. Dong, *submitted to J. Appl. Phys.*.

27. "Characterization of Electron Traps in SiO_2 as Influenced by Processing Parameters", D.R. Young, *submitted to J. Appl. Phys.*.

28. "Reduction of Electron Trapping in Silicon Dioxide by High Temperature Nitrogen Anneal", S.K. Lai, D.R. Young, J.A. Calise, F. J. Feigl, *to be published.* ***(Included in this report)***

29. "The Effects of Water on Oxide and Interface State Generation in Thermal SiO_2 Films", F.J. Feigl, D.R. Young, D.J. DiMaria, S.K. Lai, and J.A. Calise, *to be published.* ***(Included in this report).***

30. "Identification of Electron Traps in Thermal Silicon Dioxide Films", A.M. Hartstein, and D.R. Young, *to be published.* ***(Included in this report).***

31. "Hole Trapping in E-Beam Irradiated SiO_2 Films", J.M. Aitken and R. DeKeersmaecker, *to be published.* ***(Included in this report).***

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V. Papers Included in This Report

1. "Observation of amorphous silicon regions in silicon-rich silicon dioxide films", A. Hartstein, J.C. Tsang, D.J. DiMaria and D.W. Dong.

2. "Detection of Impurities in Silicon Surfaces", D.J. DiMaria, W. Reuter, D.R. Young, F.L. Pesavento and J.A. Calise.

3. "Dual Electron Injector Structure (DEIS)", D.J. DiMaria and D.W. Dong.

4. "Electrically-Alterable Memory Using A Dual Electron Injector Structure", D.J. DiMaria, K.M. DeMeyer and D.W. Dong.

5. "Radiation-Induced Trapping Centers in Thin Silicon Dioxide Films", J.M. Aitken.

6. "Attenuated total reflectance study of silicon-rich silicon dioxide films", A. Hartstein, D.J. DiMaria, D.W. Dong, and J.A. Kucza.

7. "Reduction of Electron Trapping in Silicon Dioxide by High Temperature Nitrogen Anneal", S.K. Lai, D.R. Young, J.A. Calise and F.J. Feigl.

8. "Hole Trapping in E-Beam Irradiated SiO_2 Films", J.M. Aitken and R. DeKeersmaecker.

9. "The Effects of Water on Oxide and Interface Trapped Charge Generation in Thermal SiO_2 Films", F.J. Feigl, D.R. Young, D.J. DiMaria, S. Lai and J. Calise.

OBSERVATION OF AMORPHOUS SILICON REGIONS IN SILICON RICH SILICON DIOXIDE FILMS

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ABSTRACT

Raman scattering and optical transmission measurements have been made on CVD deposited Si rich SiO_2 films (SIPOS). The measurements show seggregated regions of amorphous silicon in the as-deposited films. Annealing the films at 1150 C completely crystallizes the amorphous silicon. Annealing at lower temperatures produces films with both amorphous and crystalline regions.

Currently, there is much interest in silicon rich silicon dioxide films (commonly called semi-insulating polycrystalline silicon, SIPOS) for passivation[1,2] and non-volatile memory device[3,4] applications. Previous investigations using Auger electron spectroscopy (AES), X-ray diffraction, transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS) have shown the presence of elemental silicon and various silicon oxide phases in these films[5,6]. The exact nature of the Si regions, whether they are crystalline or amorphous, is not readily determined in these films, particularly for oxygen concentrations greater than 40%, where the silicon microcrystals, if they exist at all, are less than 10 Å in size[5]. For Si rich SiO_2 films annealed at temperatures greater than 900 C, larger microcrystals have been observed ($\leq$ 100 Å), whose size increases with annealing temperature and is only weakly dependent on oxygen concentration[5].

In this study, Raman spectroscopy has been used to show directly that as-deposited Si rich SiO_2 films, with excess Si concentrations $\leq$ 13%, contain regions of amorphous silicon which crystallize with annealing treatments. Only after annealing at 1150 C are the amorphous silicon regions completely crystallized. A transition region is shown to exist for annealing temperatures intermediate between the deposition temperature and the highest annealing temperature (1150 C). Optical transmission measurements in the visible for both as-deposited and annealed Si rich SiO_2 films support the Raman scattering results.

The Si rich SiO_2 films used in this study were chemically vapor deposited (CVD) at 700 C on both sapphire substrates to a thickness of 3000 Å and quartz substrates to a thickness of 1000 Å for the Raman and the optical transmission measurements, respectively. Using techniques previously described[7], the CVD Si rich SiO_2 layers contained 46% atomic Si and were fabricated using a ratio, R_0, of the concentration of N_2O to SiH_4 in the gas phase equal to 3. Annealing was performed sequentially at higher temperatures (800 to 1150 C) in N_2 for 30 min. with the sample surface cleaned prior to each anneal. Cleaning was performed in

alkali and acid peroxide solutions using a procedure similar to that used by Irene[8] but without HF.

The Raman spectra were excited by the 5145 Å line of an Ar^+ laser and measured in the backscattering geometry. The samples were studied at room temperature and the scattered light analyzed by a conventional double monochromator. Figure 1 shows the Raman spectra obtained from the as-deposited and annealed 3000 Å Si rich SiO_2 films. The Raman lines due to the underlying sapphire substrate have been suppressed in the figure.

The Raman spectra of crystalline and amorphous silicon (a-Si) differ considerably[9,10]. The Raman spectrum of crystalline silicon shows a single strong line at $\approx$525 cm^{-1}. This is due to scattering from the three-fold degenerate, k=0 optical phonon of Si. The Raman spectrum of a-Si shows no sharp lines for frequency shifts above 200 cm^{-1} but rather a broad assymmetric continuum peaked near 480 cm^{-1}. This continuum arises from the relaxation of the normal Raman selection rules for scattering from a crystal due to the loss of translational symmetry in the amorphous state.

In figure 1 the as-grown film and the film following an annealing step at 800 C show no evidence for any sharp line in the Raman scattering near 525 cm^{-1}. The spectra is in fact identical to that observed for amorphous silicon[9,10]. For the 1000 C anneal, and possibly for the 900 C anneal as well, we observe both the continuum scattering and the sharp line at 525 cm^{-1}. For the 1150 C anneal we observe only a single sharp line at 525 cm^{-1}. This spectrum is identical to that measured on single crystal and polycrystalline silicon.

In figure 2 we show the optical density of a 1000 Å thick film both as-deposited and following an anneal at 1000 C. The film was deposited on a quartz substrate, and the transmission was measured in a double beam spectrometer with a quartz blank in the reference beam. The optical absorption of amorphous silicon is characterized by a broad featureless continuum beginning at about 1.0 eV[11]. In contrast, the absorption of crystalline or polycrys-

talline silicon shows considerable structure in the energy region between 1 and 4 eV[11]. This structure is due to density of states effects associated with critical points in the band structure of the crystal. The loss of translational symmetry in amorphous silicon smears out this structure. We find that the annealed film shows structure which is absent in the as-deposited material. These results, combined with the Raman scattering results, strongly suggest the presence of α-Si regions in these Si rich SiO_2 films.

The Raman scattering results were checked on similar films deposited on crystal silicon substrates. The as-deposited films showed the α-Si signal, but it was not possible to repeat the annealing studies since the substrate already exhibits the crystal silicon Raman signal. Films of various thicknesses were also studied to confirm that the α-Si regions are a bulk effect and not a surface effect. Additional values of the excess silicon concentration in the films were also studied with similar results.

From these experiments we conclude that the Si rich SiO_2 films contain regions of amorphous silicon within a SiO_2 matrix. These regions are distributed throughout the bulk of the film and are quite possibly the same size ($\leq$ 100 Å) as the size of the crystal silicon regions found in the annealed films. These small amorphous silicon regions, crystallize at temperatures considerably above those required to crystallize amorphous silicon.

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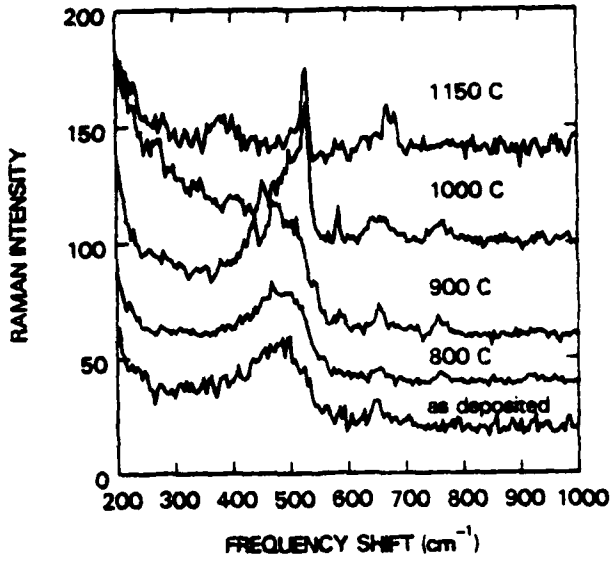

Figure 1 shows the Raman scattering spectra for Si rich SiO_2 films as-deposited and annealed at various temperatures.

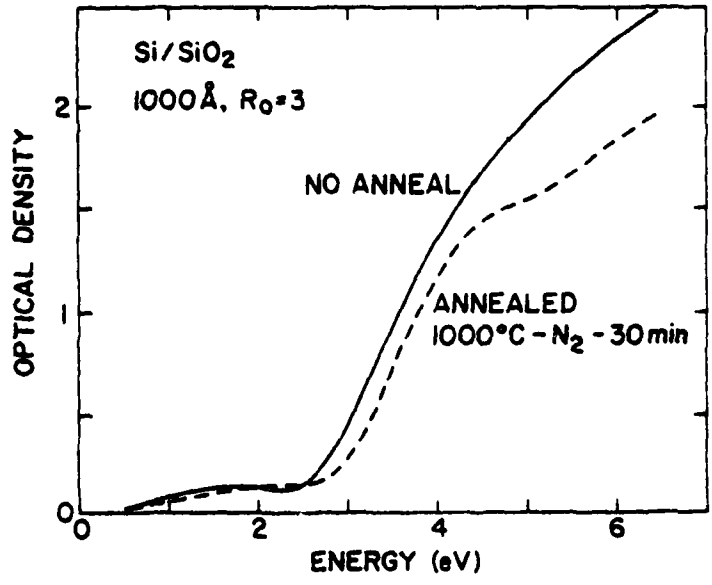

Figure 2 shows the optical density for Si rich SiO_2 films both as-deposited and following a 1000 C anneal.

Detection of Impurities on Silicon Surfaces*

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Abstract: Impurities initially present on a Si surface can be detected using the photo I-V technique. An Al impurity deposited to a thickness less than 8 Å on a silicon substrate which was subsequently oxidized, capped by a chemically vapor deposited (CVD) SiO_2 layer, and incorporated into a capacitor structure with an Al gate electrode was found mostly near the interface between the thermal and CVD oxides using the photo I-V technique. This impurity layer which was probably converted to Al_2O_3 showed greatly enhanced electron trapping compared to either oxide layer.

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Yoshino et al. have shown that the metal particle (Pt) trapping layer in dual dielectric structures composed of metal–CVD SiO_2–metal (10 Å of Pt)–thermal SiO_2–Si (MOMOS) structures can be moved relative to the Si–thermal SiO_2 interface by annealing in oxygen at temperatures between 650–850°C [1]. This was demonstrated using sputter Auger techniques which showed that the substrate Si surface was further oxidized by the annealing with the oxygen diffusing through the Pt region. This increase in the thermal oxide thickness moved the Pt layer further away from the Si–SiO_2 interface. The experiment described here is a variation of that of Yoshino et al. In our experiment, Al of $\lesssim$ 8 Å thickness is deposited directly on the Si substrate, the Si is oxidized, capped with a CVD SiO_2 layer, and then metallized for gate electrode contact. It will be shown here using the photo I-V technique [2-4] that the Al or Al converted to Al_2O_3 is found mostly near the interface between the CVD SiO_2 and thermal SiO_2. Any Al that segregates into the Si substrate during oxidation is not detected by the photo I-V technique which is sensitive to internal electric fields generated by trapped charges on impurity related sites only in the SiO_2 layer [2-4]. This Al or Al_2O_3 layer has a high trapping probability (ratio of the number of trapped carriers to the number of injected carriers) for electrons and can be easily detected using the techniques discussed in this paper. This study also demonstrates the serious problem that even a small amount of surface contaminant on an improperly cleaned Si wafer might cause in multilayer dielectric structures particularly when trapped electron build-up in the insulator is not desired. An example of this would be in field effect transistors (FETs) where a passivation layer like phosphosilicate glass or Si_3N_4 is used on top of a gate SiO_2 layer and hot electron injection effects into the SiO_2 layer from the Si surface channel or junction regions are occurring [5]. Due to the presence of the metal contaminant at the phosphosilicate or Si_3N_4 interface with the SiO_2, trapped electrons originally injected from the Si during transistor operation would build-up in the metal impurity layer and affect the operation of the transistor by the internal electric field generated by the trapped electrons.

The samples were prepared by depositing $\lesssim$ 8 Å of Al on one half of a 2 Ωcm p-Si substrate which was subsequently oxidized at 1000°C in O_2 to a thermal SiO_2 thickness of 240 Å. Then a 200 Å thick CVD SiO_2 layer was deposited at 700°C with a ratio of $[N_2O]$ to $[SiH_4]$ of 100. Following this step, surface cleaning and a 1000°C anneal in N_2 for 30 min were performed. Al gate electrodes with a thickness of 135 Å and an area of .005 cm^2 were then evaporated through a shadow mask from an rf heated crucible in a vacuum chamber under 10^{-6} Torr pressure. Finally, a post-metallization anneal in forming gas (90% N_2 and 10% H_2) gas was done at 400°C for 30 minutes to reduce surface states at the Si–thermal SiO_2 interface and reduce water-related trapping sites in the CVD SiO_2 layer. The half of the

sample which did not have the $\lesssim$ 8 Å layer of Al initially deposited on the Si will be referred to as the control structure. Electrons were injected from the Si substrate or Al gate contacts by avalanche injection of the Si [4,6] or by internal photoemission from the Si or Al [4,7]. The centroid of the trapped charge distribution was determined using the photo I-V technique [2-4]. The experimental apparatus employed in these techniques has been discussed before [4,8]. The rate of build-up of charge in the trapping layer was measured using avalanche injection with flatband voltage tracking techniques which are described in previous publications [9]. Samples were stored in an N_2 dry box when not in use. All measurements were done at room temperature.

Figure 1 shows the centroid, $\bar{x}$, of negative trapped charge in the MOMOS structures as a function of the number of trapped charges per unit area, N. From this figure, the centroid is clearly not a function of the number of trapped charges, the injecting interface (Al or Si) used to get the carriers into the oxide layers, or the type of injection used (avalanche or internal photoemission). The quantities N and $\bar{x}$ were determined from comparisons of the photocurrent as a function of gate voltage (photo I-V) characteristics before and after charging and the photo I-V relationships [2-4]. These relationships are $\bar{x}/L = (1-\Delta V_g^-/\Delta V_g^+)^{-1}$ and $N = \epsilon(\Delta V_g^- - \Delta V_g^+)/(qL)$ where L is the total stack oxide thickness, ϵ is the permittivity of SiO_2, q is the charge on an electron, and $\Delta V_g^{\pm}$ are the voltage shifts between photo I-V characteristics of samples before and after charging for positive and negative gate voltages, respectively.

Also, figure 1 shows $\bar{x}$ as a function of the increment in the number of trapped electrons, ΔN, between each charging sequence. The centroid is invariant with a value of $\approx$ 220 Å. Also, the centroid of the Al distribution which is determined using secondary ion mass spectrometry (SIMS) and the location of the CVD SiO_2-thermal SiO_2 interface (200 Å from the surface) are shown in Fig. 1. As seen in this figure, the agreement of the Al and trapped negative charge centroid positions is good with most of the Al and charge being found near the CVD SiO_2-thermal SiO_2 interface.

No electron trapping was seen on the controls (without the $\lesssim$ 8 Å Al layer) for charging conditions equivalent to those used in Fig. 1. The MOMOS structures showed a very high initial trapping probability ($\lesssim$ 1) as a result of the initial contamination of the Si substrate surface with a very small amount of deposited Al.

In Figure 2 the SIMS profiles of $^{27}Al^+$ and $^{30}Si^+$ are shown for the structure used in Figs. 1. The analysis system used in this study is described elsewhere [10]. The Al centroid

position used in Fig. 1 is deduced from the SIMS data of Fig. 2. The focused Ar^+ beam (150 μm in diameter) was raster scanned over an area of 1100 × 1200 μm accepting secondary ion signals from the central 5% of the crater only. Initial studies indicated the need for charge compensation during the course of the analysis. This was achieved by using a 30 μA 2 KeV e-beam co-aligned with the ion beam and defocused so that the flood gun covered an area slightly larger than the crater dimension. As seen in Fig. 2, the Si signal drops sharply when the SiO_2-Si interface was reached. Based on earlier studies [11], no change was expected or found in the Si signal going through an SiO_2-Si interface when using an O_2^+ beam under normal incidence. For this reason, an Ar^+ beam was used rather than an O_2^+ beam. The oxide-substrate interface was fixed at the point where the $^{30}Si^+$ value dropped to 50% of its value in the SiO_2 film.

A primary beam energy of 5 keV was used in this study in order to reduce errors in the determination of the centroid position due to cascade mixing [12,13]. This is not the optimum condition. Detailed studies of the effect of the primary beam energy on the shape of the Al distribution using a sample similar in structure, indicate a reduction in the full width at half maximum of about 15% when the primary beam energy is reduced from 5 to 3 keV. Further reduction of the primary beam energy to 2 and 1.5 keV results in no further reduction of the full width at half maximum. Over the same energy range the centroid position shifts towards the center of the oxide structure by 5%. A correction for this centroid shift would make the agreement between SIMS and the photo I-V data even better. However, this correction was not made in Fig. 1 because the energy dependent study was not made on the identical sample.

Some of the physical properties of electron trapping and detrapping in this buried impurity layer were measured using well established techniques such as capacitance-voltage (C-V) and photocurrent-voltage (photo I-V) [2-4]. The buried impurity layer is probably mostly Al_2O_3, but some microscopic Al regions might still exist. Also, some regions with a physical character similar to trapping sites in Al ion-implanted SiO_2 could be present. However, as will be discussed next, the physical properties that were measured could not easily differentiate between these three different possibilities for the microscopic nature of the buried impurity layer. The number of electron traps was very large, $\lesssim 10^{13}$ cm^{-2}, with capture cross sections $\lesssim 10^{-13}$ cm^2. In contrast to trapped electrons on sites related to ion implanted Al [9, 14-16], most of the trapped electrons on these sites could be optically discharged with energies from 3-5 eV. The threshold energy for photoionization was $\approx$ 3 eV. Photoionization cross-sections were 10^{-18}–10^{-17} cm^2 in the energy range from 3 to 5 eV. This 3 eV threshold (photoexcitation from traps to SiO_2 conduction band) is comparable to the $\approx$ 3 eV

electronic energy barrier observed for the interface of an Al gate electrode on SiO_2 [4] (photoexcitation from the Al Fermi level to the SiO_2 conduction band). This 3 eV threshold is also consistent with photodetrapping of electrons from traps in Al_2O_3 [17,18]. Trapped electrons in this buried Al or Al_2O_3 layer could be thermally discharged at temperatures $\gtrsim$ 150°C with rates in line with a median thermal trap energy of 1.2-1.3 eV [19] which is consistent with what is expected for an optical threshold of $\approx$ 3 eV [19]. Traps related to ion implanted As and P have similar optical and thermal threshold energies [4,19,20].

To exaggerate the effect of surface contamination, an Al layer of $\lesssim$ 8 Å in thickness (corresponding to $\lesssim 5 \times 10^{15}$ atoms/cm^2) was deposited on the Si surface. However, using the characterization techniques described here (photo I-V and avalanche injection with flat-band voltage tracking) which are sensitive to charges trapped on impurity related sites in SiO_2, parts-per-million detection is possible for 1000 Å thick films. The detectability of ion implanted Al or As fluence levels of 3×10^{12} ions/cm^2 has been experimentally demonstrated in previous publications [9,19]. This corresponds to a volume density of $\approx 10^{17}$ to 10^{18} ions/cm^3 for a 1000 Å thick film of SiO_2 which is ten to one hundred parts per million detection for an SiO_2 density of 2.3×10^{22} molecules/cm^3. However, the ultimate level of detectability using these electrical characterization techniques is at least one part per million for SiO_2 films of $\approx$ 1000 Å in thickness as has been shown for uniformly-distributed radiation-induced neutral trapping centers [21]. For very thick SiO_2 layers ($\gtrsim$ 1 μm), parts-per-billion uniformly-distributed H_2O-related impurity levels can be detected using these electrical techniques [22]. However, any impurity which gives a photo I-V voltage shift of $\approx$ 0.5 V due to the presence of trapped charges is detectable [21]. For example, a photo I-V voltage shift of .5 V due to uniformly-distributed, bulk-SiO_2 trapped charges gives a volume density $n = 8.6 \times 10^{12}$ trapped charges/cm^3 (parts-per-billion detectability) and an areal density of 4.3×10^9 cm^{-2} in a 5 μm thick SiO_2 film. For a 1000 Å thick SiO_2 film, a .5 V shift gives a volume density of 2.2×10^{16} cm^{-3} (parts-per-million detectability) and an areal density of 2.2×10^{11} cm^{-2}. These numbers were calculated using the photo I-V relationship $N = \varepsilon(\Delta V_g^- - \Delta V_g^+)/(qL)$ where $\Delta V_g^+ = -\Delta V_g^- = 0.5$ V and $N = \int_0^L n(x)dx = nL$ for uniformly distributed SiO_2 charges. Films much thicker than 10 μm are difficult to fabricate due to stress-related problems at the Si-SiO_2 interface. This limits the ultimate sensitivity of techniques discussed here to about the parts-per-billion level.

The results of Figs. 1 and 2 show that most of the Al layer initially deposited on the Si surface has been moved out to near the thermal-SiO_2 – CVD-SiO_2 interface by the thermal oxidation. The oxygen probably converted this layer to Al_2O_3 before oxidizing the underlying Si surface by diffusing through this very thin Al_2O_3 layer. This interfacial layer when

surrounded by SiO_2 on either side acts as a very effective trapping site. In fact, all the experimental results were very similar to those for MOWOS structures where a thermal oxide was grown first, tungsten less than a monolayer thick evaporated onto its surface, and then a CVD SiO_2 capping layer deposited [2,23-26].

The results presented in this paper, together with the detectability limits of the techniques used here which have been demonstrated in previous publications [9,19,21,22], imply that trace amounts of contaminants introduced on Si wafer surfaces during cleaning can be detected quickly and easily in a non-destructive manner. On very thick SiO_2 layers ($\gtrsim$ 1 μm), these electrical characterization techniques are capable of parts per billion impurity sensitivity for approximately uniformly-distributed SiO_2 impurities which trap charges [22]. This is not possible with any other technique such as SIMS, Auger, ESCA, or RBS. However, techniques such as SIMS and RBS do give unequivocal determination of the impurity atoms whereas the electrical characterization techniques are indirect and depend upon existing characterization data (capture cross sections, photoionization cross sections, etc. [4]) for the determination of trapping sites related to the impurity atoms. If the impurities initially present on the Si surface mostly segregate into the Si substrate during oxidation, or if they do not have electron or hole capture probabilities larger than those of the sites normally present in the SiO_2 [4], then the techniques used here will not be very effective.

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FIGURE CAPTIONS

Fig. 1. Ratio of the centroid to total oxide thickness ($\bar{x}/L$) as a function of either the number of trapped charges per unit area (N) or the increment in the number of trapped charges per unit area (ΔN) for several samples. Electrons to fill traps in the Al or Al_2O_3 region were injected by either internal photoemission from the Al at a light energy of 4.5 eV and gate voltages from -7 to -16 V or by avalanche injection from the Si substrate at a constant current of 2×10^{-10} A. The uncharged sample was the virgin as fabricated structure. For $\bar{x}/L$ as a function of ΔN, the comparison of the photo I-V data was made between a charged sample before and after it was charged further. Solid symbols refer to experimental data for $\bar{x}/L$ as a function of N, while open symbols refer to $\bar{x}/L$ as a function of ΔN. The solid line represents $\bar{x}/L$ for the Al profile determined using the SIMS data in Fig. 2 and the dashed line represents the position, normalized to L, of the CVD SiO_2 and thermal SiO_2 interface. All centroids (trapped charge and Al) and the interface position are measured from the top surface of the CVD SiO_2 or the interface of this top surface of the CVD SiO_2 with an Al gate electrode.

Fig. 2. SIMS profile of $^{27}Al^+$ and $^{30}Si^+$ as a function of distance from the top SiO_2 surface on the same sample as used in Fig. 1. An electron flood gun was used for charge compensation.

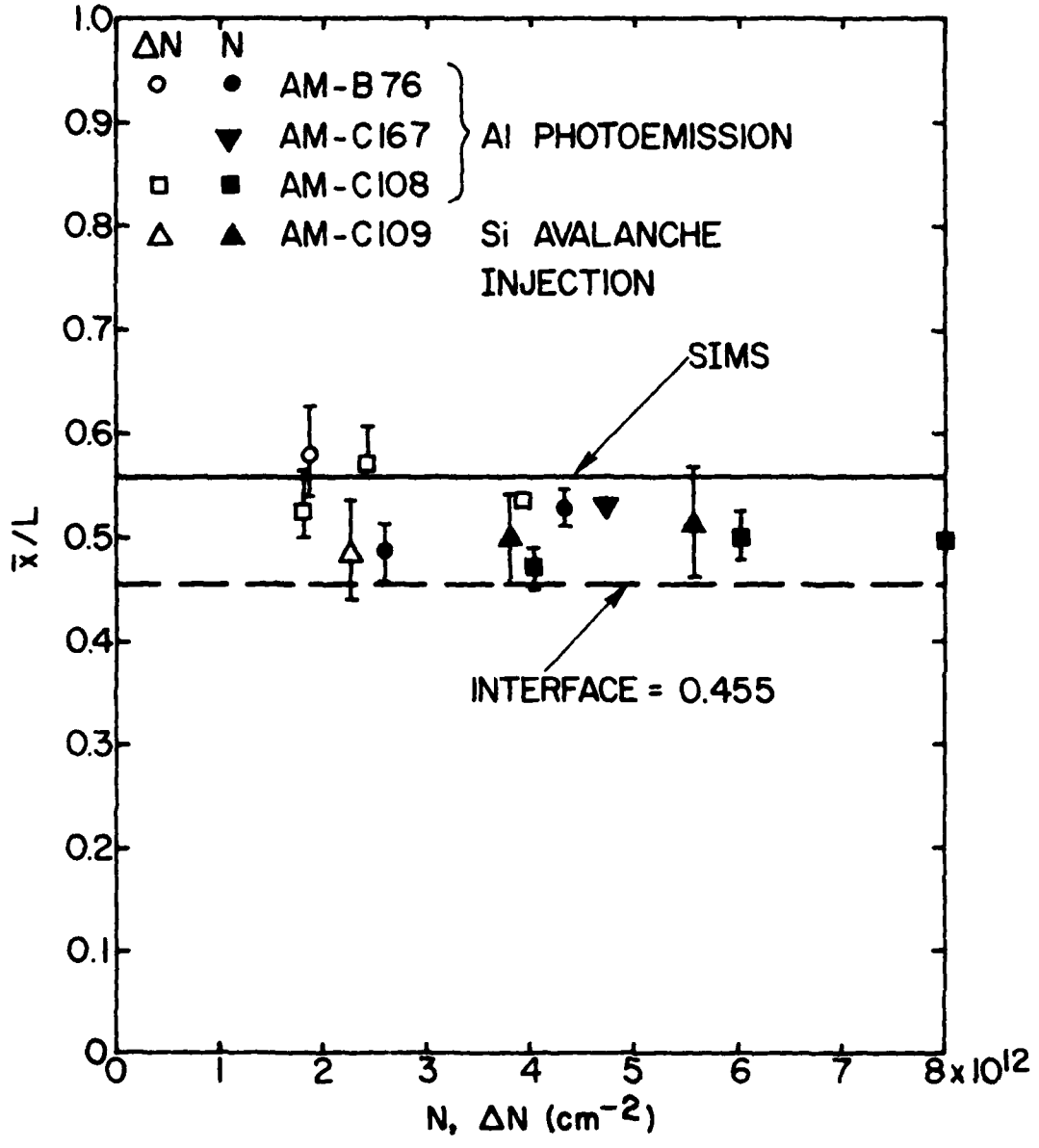
ΔN N
AM-B76
AM-C167
AM-C108
Al PHOTOEMISSION
AM-C109
Si AVALANCHE INJECTION
SIMS
INTERFACE = 0.455
x̄/L
N, ΔN (cm⁻²)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
4
5
6
7
8x10¹²

FIGURE 1

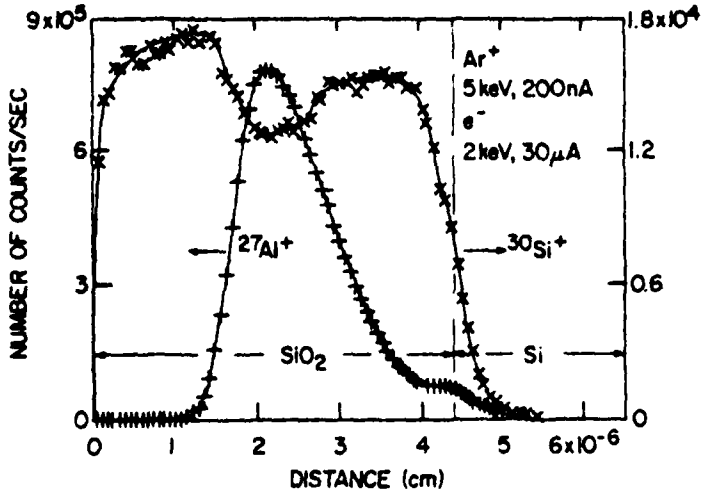
9x10^5
6
3
0
1.8x10^4
1.2
0.6
0
NUMBER OF COUNTS/SEC
Ar+
5keV, 200nA
e-
2keV, 30μA
27Al+
30Si+
SiO2
Si
0
1
2
3
4
5
6x10^-6
DISTANCE (cm)

FIGURE 2

Dual Electron Injector Structure (DEIS)

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Abstract: Experimental results are presented which show for the first time that stacked chemically-vapor-deposited insulator combinations such as Si rich SiO_2 - SiO_2 - Si rich SiO_2 sandwiched between Si or metal electrodes can be tailored to give any desired injection current characteristic for positive and negative voltage biases. The Si rich SiO_2 - SiO_2 interfaces give enhanced electron injection into the SiO_2 layer. By modifing this interface and the Si rich SiO_2 layer (for example, by changing its Si content), current as a function of voltage characteristics for each of the two interfaces of the Si rich SiO_2 injecting material with the SiO_2 layer can be modified as desired. These dual electron injector structures (DEIS) are discussed with respect to optimizing the write and erase characteristics of non-volatile semiconductor memories using a floating polycrystalline silicon storage layer with a DEIS sandwiched in between it and a control gate.

* This research was supported by the Defense Advanced Research Projects Agency, and was monitored by the Deputy for Electronics Technology (RADC) under *Contract No. F19628-78-C-0225*

Recent publications have demonstrated that Si rich SiO_2 layers deposited on top of SiO_2 give large electron current injection into the SiO_2 at moderate electric fields [1,2]. Also in these articles, the feasibility for using these layers in non-volatile semiconductor memories has been shown. However, since the Si rich SiO_2 layers are only a good single carrier electron injector and few holes are injected for the opposite polarity, the "erase" times are long (mins) compared to the "write" times (msecs) [2]. This letter presents a solution to the erasure problem by using stacked chemically-vapor-deposited (CVD) layers of Si rich SiO_2 - SiO_2 - Si rich SiO_2 between the control gate (Al or polycrystalline Si (poly-Si)) and the charge trapping layer (floating poly-Si) used for memory storage in most non-volatile semiconductor memory devices. This insulator stack will be referred to as a dual electron injector structure (DEIS). Since a negative voltage bias on the control gate injects electrons onto the floating gate and a positive voltage bias pulls them back to the control gate as shown in Fig. 1, the electrons are injected at moderate SiO_2 electric fields into this intervening oxide layer by means of the Si rich SiO_2 injector which is at the lower potential. This injection phenomena (for a single injector on top of SiO_2) is believed to be due to localized electric field distortion at the Si rich SiO_2 - SiO_2 interfaces [2].

The DEIS structures and their controls were formed by depositing CVD Si rich SiO_2 and SiO_2 layers on top of (100) 2 Ω cm p-type single crystal Si substrates at 700°C. The ratio, R_o, of the concentration of N_2O to SiH_4 in the gas phase was varied in the range from 10 to 3 (7% to 13% excess atomic Si over stoichiometric SiO_2, respectively) for the Si rich SiO_2 injectors [3] and R_o = 100 for the CVD SiO_2 layers. Thick (1 micron) Al electrodes with an area of .006 cm^2 were deposited next, followed by a forming gas (90% N_2 - 10% H_2) anneal at 400°C for 20 min.

All DEIS structures were evaluated for electron injection using current as a function of ramped gate voltage (ramp I-V) techniques [4]. A Keithley #26220 logarithmic picoammeter was used to measure the current with a voltage source that had adjustable ramp rates. For positive gate voltage ramp I-V experiments, the Si inversion layer was maintained to prevent any significant voltage from being dropped across the Si by shining white light on the sample. This white light, although shielded by the thick Al gate electrode, provides minority carriers (electrons) around the periphery of the depletion layer formed under the positively biased Al gate electrode. These electrons subsequently diffuse laterally and form the inversion layer. In all experiments, a virgin as-fabricated location was used for each I-V characteristic for which the gate voltage was ramped from 0 V at a rate of −.47 V/sec or +.47 V/sec to the desired value.

The data of Figs. 2-4 demonstrate the dual electron injector concept. Fig. 2 and Fig. 3 show a single injector in between the Al gate electrode and SiO_2 layer, and Si substrate and SiO_2 layer, respectively. Comparing Figs. 2 and 3, enhanced electron injection is seen from the electrode with the single injector next to it when this electrode is biased at a lower potential than the opposite electrode. The smaller electron currents in Figs. 2 and 3 are due to Fowler-Nordheim tunneling through an $\approx$ 3 eV interfacial energy barrier at the Si or Al interface with the SiO_2 layer [5]. The larger current in each of these figures is throught to be due to field-enhanced Fowler-Nordheim tunneling at the Si rich SiO_2 - SiO_2 interface due to the two phase (Si and SiO_2) nature of the Si rich SiO_2 material [2]. Because of the high conductivity of the Si rich SiO_2 compared to SiO_2, only a small fraction of the total applied voltage is dropped across this layer [2-4]. Figure 4 shows the total DEIS stack with a CVD injector near each interface separated by the CVD SiO_2 layer. The measured currents in Fig. 4 are approximately equal to the appropriate enhanced currents due to the Si rich SiO_2 injector in Figs. 2 and 3 for negative Al gate voltage bias (Fig. 2) and positive Al gate voltage bias (Fig. 3). There are two current ledges in the data of Figs. 2-4. The low current ledge at $\approx 3 \times 10^{-10}$ A is due to a displacement current term which is equivalent to the total insulator stack capacitance multiplied by the voltage ramp rate. The current ledge at $\approx 10^{-7}$ A is due to trapping occurring in the CVD SiO_2 layer [4]. This trapping ledge which is believed to be due to the presence of H_2O in the films [4] is removed with high temperature annealing (1000°C for 30 min. in N_2 or forming gas) prior to gate metallization. From the approximately equivalent position and width of these ledges for either polarity for the DEIS of Fig. 4, the centroid is deduced to be approximately half way into the CVD SiO_2 layer [4]. The reduction in ledge width in the ramp I-V data for positive polarity in Fig. 2 and negative polarity in Fig. 3 where current enhancement is absent (no injector present) is thought to be due to field ionization of the trapped electrons or reduction in the trapping rate [4].

The voltage reduction factor for electron injection from the Si substrate side was smaller than the voltage reduction factor for electron injection from the Al side. The voltage reduction factor, defined as the ratio of the gate voltage with a Si rich SiO_2 injector to that without the injector required to obtain a given current, was approximately 1/2 and 2/3 for electron injection from the Si and Al sides, respectively. Although presumably equivalent Si rich SiO_2 injectors were deposited (100 Å thickness using R_o = 3 material), the SiO_2 - Si rich SiO_2 interfaces for the DEIS structure in Fig. 4 could be different since for the Si side the SiO_2 is deposited on the injector and for the Al side the injector in deposited on the SiO_2.

The electron injection characteristic of either injector in Fig. 4 could be changed by modifying the Si content of the Si rich SiO_2 layers. Injectors with less excess Si have smaller

current enhancements (voltage reduction factors closer to 1) and more of the applied voltage is dropped across their layers. Modifying one injector of a DEIS so that more voltage is dropped across it will change the I-V characteristic of the other injector somewhat. Since this unmodified injector and the intervening oxide see a smaller fraction of the total applied voltage bias, the I-V characteristic for this injector will have a particle current threshold above the displacement current level at a larger magnitude of the applied bias, and the I-V characteristic will have a shallower slope.

This paper clearly shows how a desired I-V characteristic can be obtained for each voltage polarity by stacking the appropriate insulators between the contacts. Write and erase characteristics of non-volatile semiconductor memories employing floating poly-Si storage layers and DEIS stacks between the control gate and floating poly-Si can be tailored separately, both being independent of the read operation which is controlled by a surface channel in the substrate Si.

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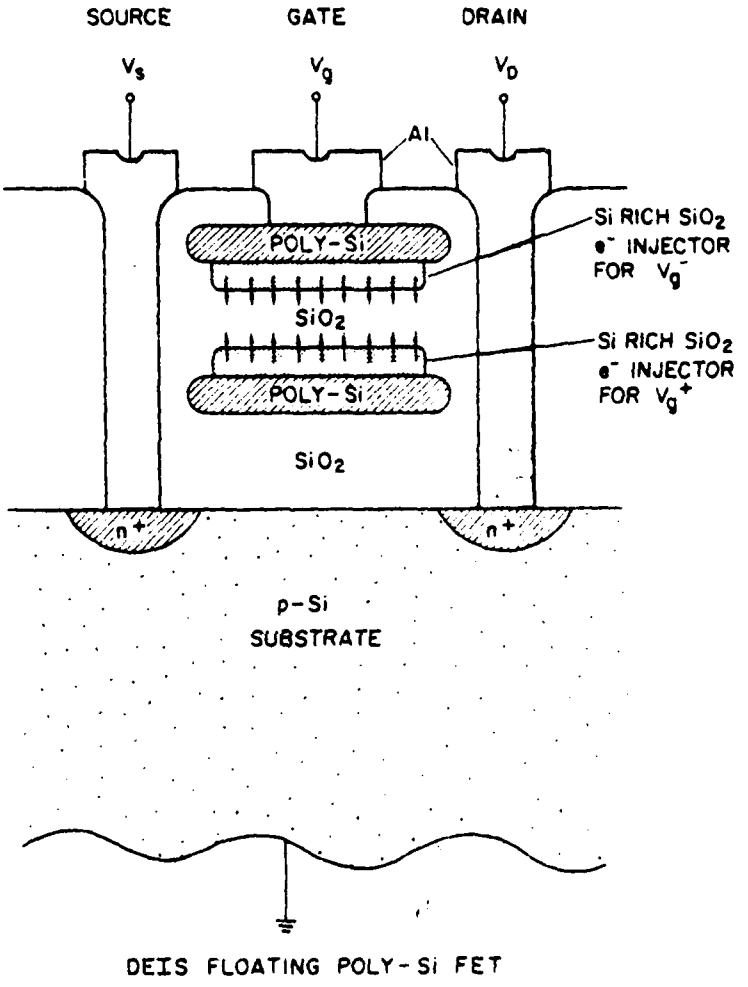
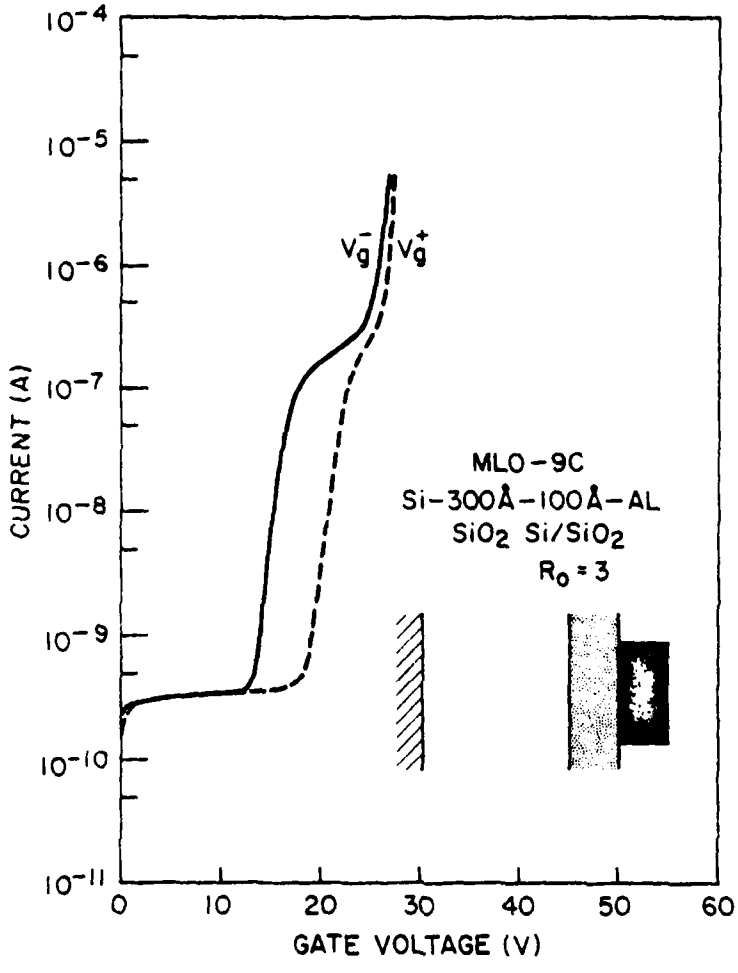


Figure 1 Schematic representation of a non-volatile n-channel field effect transistor memory using a dual electron injector stack between a control gate and floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage, $Vg^-(Vg^+)$, to the control gate which injects electrons from the top (bottom) Si rich SiO_2 injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale.



gure 2 Magnitude of the dark current as a function of the magnitude of the gate voltage for a single Si rich SiO_2 injector on top of the SiO_2 layer where this injector is under the Al gate electrode. A virgin as-fabricated sample was ramped from 0 V at +.47 V/sec or −.47 V/sec for positive gate voltage (V_g^+) or negative gate voltage (V_g^-).

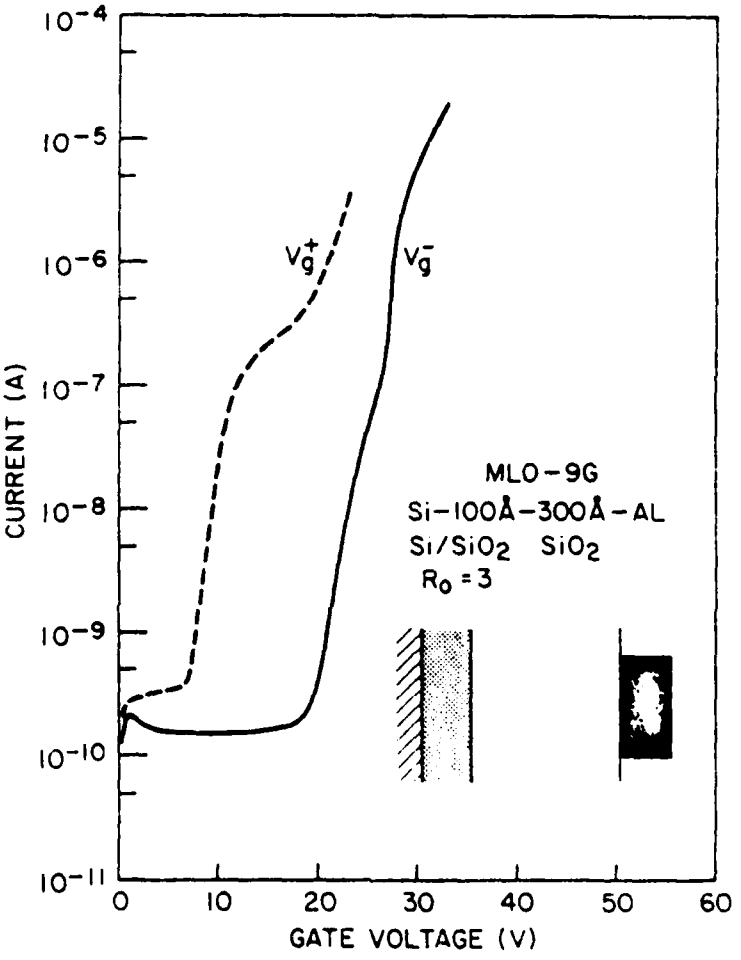


Figure 3 Magnitude of the dark current as a function of the magnitude of the gate voltage for a single Si rich SiO_2 injector under the SiO_2 where this injector is on top of the Si substrate. Same experimental conditions as in Fig. 2 were used.

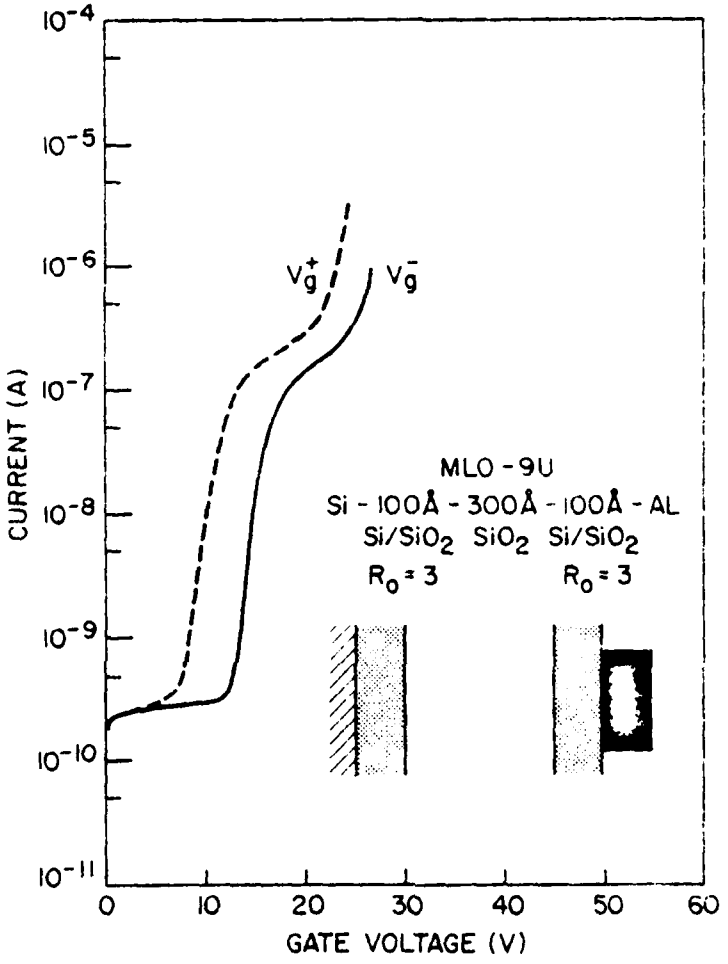


Figure 4 **Magnitude of the dark current as a function of the magnitude of the gate voltage for a dual Si rich SiO_2 injector structure which is essentially the sum of those characteristics in Figs. 2 and 3 for the same SiO_2 thickness. Same experimental conditions as in Fig. 2 were used.**

Electrically-Alterable Memory Using A Dual Electron Injector Structure*

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ABSTRACT: A novel type of electrically-alterable memory which uses the phenomenon of enhanced electron injection into SiO_2 from Si-rich SiO_2 to charge or discharge a floating polycrystalline Si storage layer in a metal-oxide-semiconductor field-effect-transistor is described. This non-volatile memory differs from others using floating polycrystalline Si in the charging or discharging process. This improvement is accomplished by using a chemically-vapor-deposited stack of Si-rich-SiO_2–SiO_2–Si-rich-SiO_2 between the floating polycrystalline Si layer and the control gate electrode. This device is capable of being written or erased in 5 msec at voltages $\lesssim$ 16 V and in 2 μsec at voltages $\lesssim$ 23 V with excellent charge retention.

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In this communication, a new non-volatile electrically-alterable read-only-memory (EAROM) is described which uses a floating polycrystalline silicon (poly-Si) storage layer [1] and Si-rich SiO_2 electron injectors [2-4]. This device, as shown schematically in Fig. 1, is similar to commercially available floating-gate avalanche-injection metal-oxide-silicon (FAMOS) devices [1] except for the replacement of the SiO_2 layer between the floating poly-Si layer and control poly-Si electrode by a dual electron injector structure (DEIS) consisting of sequentially chemically-vapor-deposited (CVD) layers of Si-rich SiO_2, SiO_2, and Si-rich SiO_2. The DEIS allows the floating poly-Si layer to be written or erased by putting electrons on or taking them off this storage layer using enhanced electron injection from the top or bottom Si-rich SiO_2 injectors, respectively. The enhanced electron injection phenomenon is thought to be caused by localized electric field enhancement at the Si-rich-SiO_2–SiO_2 interface due to the two phase nature (Si and SiO_2) of this material [2,3]. This localized field distortion gives a very large enhancement ($\gtrsim 10^5$) in the injected current for a given gate voltage which is believed to be controlled by Fowler-Nordheim tunneling [2,3]. In contrast, commercially available FAMOS structures are written by hot electron injection from a Si junction pulsed to avalanche breakdown and usually rather slowly erased by ultra-violet (UV) light which optically discharges the trapped electrons on the floating poly-Si storage layer [1]. As will be demonstrated here, the DEIS EAROM can be both written and erased in $\lesssim$ 5 msec at least 10^4 times with very little degradation, using lower voltage and power than FAMOS type structures but with similar retention characteristics. The DEIS EAROM can also be written and erased at lower voltages than metal-silicon nitride-silicon dioxide-silicon (MNOS) devices which depend on electron and hole tunneling (write and erase operations, respectively) from the Si substrate through a thin tunnel SiO_2 layer into the Si_3N_4 layer which stores the charge via trapping states lying energetically in the bandgap [5]. Furthermore, the DEIS like the FAMOS structures has better charge retention characteristics than MNOS devices.

The EAROM n-channel field effect transistors (FETs) used here were fabricated using a self-aligned, double poly-Si process with a DEIS stack deposited between the poly-Si layers.

The FET channel area was 2.9×10^{-6} cm^2, but the actual injecting area was 8.4×10^{-6} cm^2. To increase the capacitive coupling effect so that most of the applied voltage is dropped across the DEIS stack, the thermal gate oxide between the Si substrate and the floating poly-Si layer was made thin (100 Å). Although in the devices described here the poly-Si control gate electrode and floating gate storage electrode are equal in area, higher coupling also could have been realized with a control gate which was smaller in area than the floating poly-Si layer. The DEIS stack consisted of 100 Å of Si-rich SiO_2 for the bottom injector, 100 Å of SiO_2 for the intervening oxide layer, and 100 Å of Si-rich SiO_2 for the top injector. The Si-rich SiO_2 and SiO_2 layers were deposited at 700°C using concentration ratios R_o of N_2O to SiH_4 in the gas phase of 3 and 100, respectively [2,3,6]. This Si-rich SiO_2 material with R_o=3 has 46% atomic Si [2,3,6].

Figures 2 and 3 show write/erase cycling data for 5 msec and 2 μsec pulse widths, respectively. In Fig. 2 for 5 msec operation, write voltages were varied from -14 V to -16 V while erase voltages were varied from +11 V to +13 V. In Fig. 3 for 2 μsec operation, write voltages were varied from -20 V to -23 V, while erase voltages were varied from +17 V to +20 V. The threshold voltage indicates the charge state of the floating poly-Si layer with the horizontal dashed line indicating the initial threshold voltage on an approximately uncharged as-fabricated device. Threshold voltages more positive than this dashed line indicate stored electrons, while those more negative indicate ionized donors when the device is over-erased. The degradation in the cycling characteristics resulting in a threshold-voltage window collapse which becomes important after approximately 10^4 cycles is due to trapped electronic charge build-up in the intervening CVD SiO_2 layer [3,7]. This trapping is believed to be caused by H_2O related impurities in these films [3,7,8] and can be improved with high temperature annealing [3,7].

Figures 2 and 3 also show that the erase operation (electron ejection from floating poly-Si back to the control gate using the bottom Si-rich SiO_2 injector) is more efficient than the write

operation (electron injection from the control gate to the floating poly-Si using the top Si-rich SiO_2 injector). This same phenomenon was also seen on large area (.006 cm^2) capacitor structures with DEIS stacks deposited on smooth single crystal Si or rough poly-Si substrates with poly-Si or Al control gate electrodes [4,9]. This asymmetry in the enhanced currents from the Si-rich SiO_2 injectors is believed to be caused by differences in the two Si-rich-SiO_2–SiO_2 interfaces [4]. The bottom injector interface is formed by depositing SiO_2 on top of it, while the top interface is formed by depositing the top injector on top of this SiO_2 layer.

Control structures identical to the DEIS EAROMs discussed here with only the 100 Å CVD SiO_2 layer between the control gate and floating poly-Si were also fabricated. These structures could not be written with any significant number of electrons using the same voltages and times in Figs. 2 and 3. However, they could be erased somewhat due to localized field-enhanced tunnel injection near asperities on the rough top surface of the floating poly-Si storage layer [10,11]. This phenomenon has been reported before and actually used with FAMOS-like devices in some cases for erase operations [12]. However, it is very difficult to reproduce due to subtleties in processing conditions effecting the surface roughness.

Figure 4 shows retention characteristics of the DEIS EAROMs in a grounded control gate condition for temperatures in the range from 25°C to 300°C and compares them to control structure EAROMs for approximately 3×10^{12} stored electrons/cm^2. Clearly, the DEIS and control structure without the Si-rich SiO_2 layers behave in a very similar fashion. Temperatures of 300°C are needed to observe any significant charge loss in 10^4 sec. This loss has been shown to be due to electronic thermal activation out of an approximately 2.2 eV energetically deep well formed by the electric field lowered energy barrier between the Fermi level of the n-degenerate poly-Si storage layer of the control structure or the bottom of the conduction band of the last layer of Si islands in the bottom injector of the DEIS and the conduction band of the CVD SiO_2 layer [9]. If large enough positive gate voltages are applied

to the DEIS EAROM, another loss component which is weakly temperature dependent will occur during the times considered here [9]. This is due to Fowler-Nordheim tunneling of electrons off the last layer of Si islands in the bottom Si-rich SiO_2 injector into the CVD SiO_2 layer (the injector starts ejecting electrons back to the control gate). This loss mechanism will also occur at higher positive gate voltages on the control EAROM structure in a localized fashion from near the tips of the asperities on the rough poly-Si surface into the intervening CVD SiO_2 layer. From the higher temperature data in Fig. 4, a 5% charge loss in $\gtrsim 10^7$ years by thermal activation is predicted for DEIS EAROM operation at temperatures from 25°C to 80°C. The principal charge loss mechanism over periods of years will be by Fowler-Nordheim tunneling. However, this process will be self-limiting since as electrons are lost off the floating gate the internal electric fields which drive this loss component will decrease [9].

Other sets of devices similar to those reported here with thicker SiO_2 layers were also fabricated. They operated in a similar fashion to those reported here, but at higher voltages. Varying the Si-rich SiO_2 injector thickness from 100 Å to 500 Å or the Si content by a few percent from the 46% atomic Si used here had little effect on write/erase operation making the DEIS processing non-critical. Write or erase voltages could be increased by significantly decreasing the Si content of the Si-rich SiO_2 injectors either separately or together. If either the top or bottom injector is replaced by SiO_2, the expected behavior of enhanced injection only from the remaining injector is observed [4]. The sum of the current-voltage characteristics of structures with a single top or bottom injector has been shown to be approximately equivalent to the current-voltage characteristic for a DEIS with the same SiO_2 thickness [4]. The DEIS stacks have also been shown to have excellent voltage breakdown characteristics, and they are capable of drawing very high currents as would be needed for the 2 μsec operation shown in Fig. 3 with very few low voltage breakdown events occurring [9]. This phenomenon is believed to be due to localized field screening by a reversible space charge build-up on the Si islands near the injecting contact at low applied fields [9,13]. In fact, even 200 nsec write/erase operation for 10^2 to 10^5 cycles depending on the magnitude of the

voltage pulses has been demonstrated for these devices before the gate insulator between the floating poly-Si layer and the single crystal Si substrate broke down.

Smaller area FETs using capacitive coupling considerations will allow even lower voltages and faster write/erase switching times than those reported here. In the future, $\lesssim$ 100 nsec write/erase operation at $\approx$ 20 V should be attainable. If oxide trapping can be reduced significantly so that the number of cycles before a pronounced threshold-voltage window collapse is increased to $\gtrsim 10^9$, then a pure non-volatile Random-Access-Memory (NVRAM) structure might finally be obtained.

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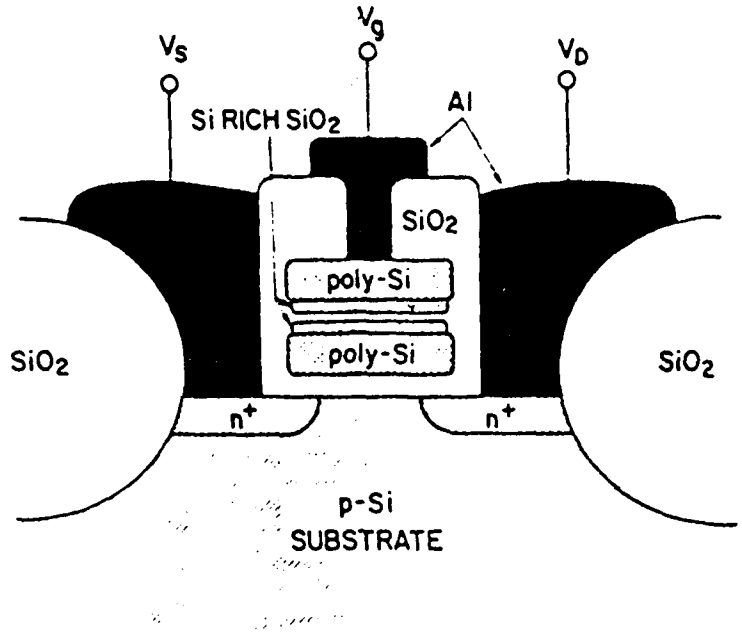

Figure 1. Schematic representation of a non-volatile n-channel field effect transistor memory using a dual electron injector stack between a control gate and floating poly-Si layer. Writing (erasing) is performed by applying a negative (positive) voltage $V_g^-(V_g^+)$, to the control gate which injects electrons from the top (bottom) Si-rich SiO_2 injector to the floating poly-Si storage layer (back to the control gate). Structure is not drawn to scale.

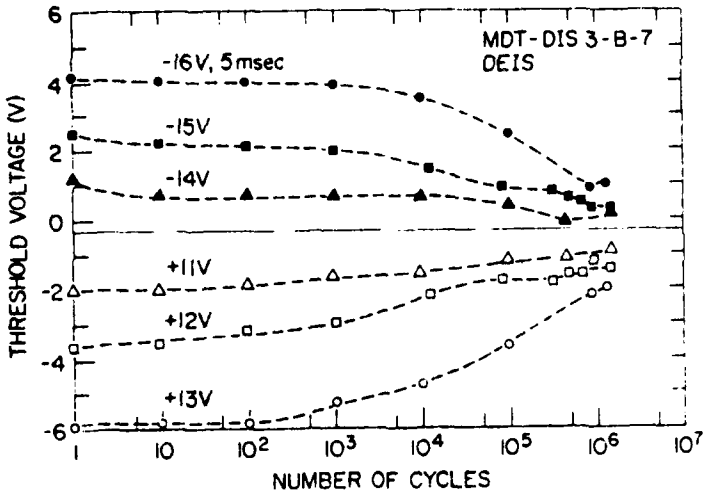

Figure 2. Threshold voltage after writing and erasing as a function of the number of cycles for various write/erase voltage conditions on DEIS FETs from wafer *MDT-DIS 3-B, as described in the text of this communication. Solid and open* symbols correspond to the threshold voltage after writing and erasing for 5 msec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling.

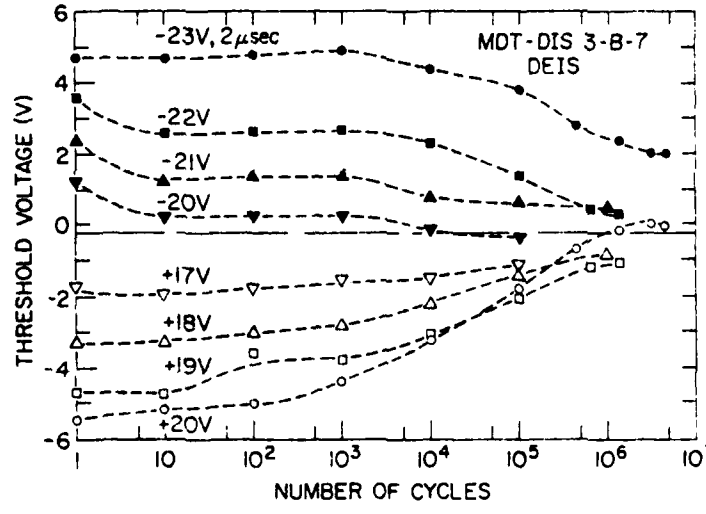

Figure 3. Threshold voltage after writing and erasing as a function of the number of cycles for various write/erase voltage conditions on DEIS FETs from wafer MDT-DIS 3-B. Solid and open symbols correspond to the threshold voltage after writing and erasing for 2 μsec, respectively. The horizontal dashed line indicates the initial threshold voltage of the as-fabricated FETs before cycling.

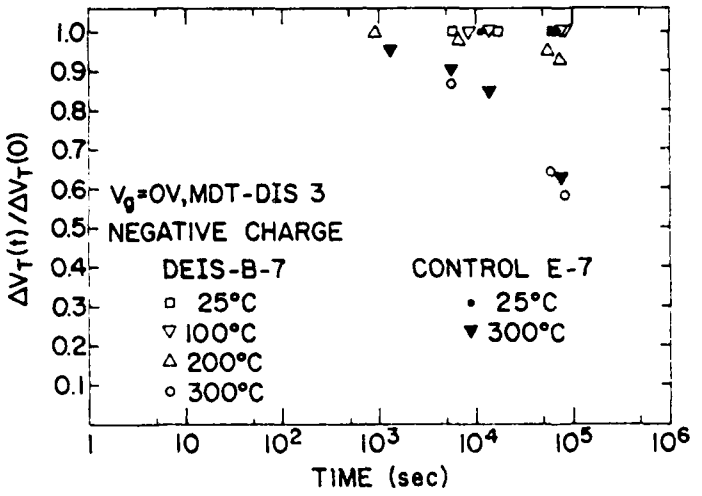

Figure 4. Stored electronic charge loss as a function of time on DEIS and control FETs from the MDT-DIS 3 series as described in the text of this communication for a grounded gate condition V_g=0 V at temperatures of 25°C, 100°C, 200°C, and 300°C. Charge loss is calculated in normalized units of $\Delta V_T(t)/\Delta V_T(0)$ where $\Delta V_T(0)$ is the threshold voltage shift due to the initial stored charge of $\approx 3x10^{12}$ electrons/cm^2 and $\Delta V_T(t)$ is the threshold voltage shift due to the stored charge left after time t under the indicated temperature and voltage stressing conditions.

RADIATION-INDUCED TRAPPING CENTERS IN THIN SILICON DIOXIDE FILMS

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Abstract: In this paper the technologic and scientific aspects of radiation-related charge trapping in thin SiO_2 films are reviewed. These films are amorphous in nature and are thermally grown on single crystal silicon substrates serving as the insulating layer in Metal-Oxide-Semiconductor (MOS) capacitors and transistors. The structure and operation of these devices are reviewed with special emphasis on the effect of charges trapped in the oxide. The technical importance of understanding the interaction of ionizing radiation with thin SiO_2 films is illustrated with two practical examples. The first involves the operation of MOS transistors in environments where ionizing radiation is present, leading to an accumulation of positive space charge in the oxide. The second deals with process-induced defects generated by radiation encountered during the fabrication of devices by processes such as electron beam lithography or electron gun metallization. Unannealed traps of this type capture hot electrons produced in the substrate during the operation of the MOS transistor. In both these examples, the charging of the oxide results in instabilities which degrade operation.

Its sensitivity to charge trapped in the insulator makes the MOS system an ideal vehicle for scientific study of these phenomena. The basic techniques for characterizing the density, capture cross-sections, and location are briefly discussed and applied to the problem of radiation-induced defects in thin SiO_2 films. Ionizing radiation is shown to interact with the SiO_2 in two modes. In the first it supplies carriers to fill pre-existing hole traps at the interfaces. In the second it creates electron and hole traps in the bulk of the thin film. These latter defects are in a neutral state after irradiation and are detectable only when either electrons or holes are subsequently injected into the oxide. The capture cross-sections, trap densities and location of these centers in the film are presented. The annealing treatments required to remove these traps from aluminum and polysilicon gate devices are also discussed. The number of traps produced by an incident 25KV electron beam is found to depend weakly on the dosage. A dipolar defect, produced by the ionizing radiation, seems to explain the behavior of the neutral centers.

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INTRODUCTION

Thin silicon dioxide films play a fundamental role in modern microelectronic technology[1]. The rapid progress in this industry in recent years is partly due to the versatility of these films. They define the structure of the device itself by acting as diffusion/implantation or etching masks. They isolate active devices on the surface of the semiconductor from each other. They passivate the active device areas against contaminants such as moisture or mobile ions which affect operation. In Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET's) ,these films play an important additional role. By serving as gate oxides, SiO_2 films are an active part of the device operation. They capacitively couple control voltages applied to the contact to the underlying semiconductor and modulate its conductivity[2,3]. The principle of this device was postulated 30 years before a working device was made[4]. Actual devices were possible only with the advent of modern SiO_2 thin film technology. The remarkable dielectric strength, high purity, and stability of these films make them the cornerstone of MOSFET technology.

A simple n-channel MOSFET structure is shown in Fig. 1. The spacing between source and drain diffusions is typically from 1 to 5um. The isolation oxide is around 0.5 to 1 um thick while the gate oxide is between 25 and 100 nm thick. Other embodiments of this device are commonly used and discussed in detail elsewhere[2] However the role of the gate oxide is the same in all MOSFET structures and can be illustrated using this particular n-channel enhancement mode device as an example. Electrons in the heavily doped n-type source and drain regions are separated physically and electrically from each other by a p-doped semiconducting region called the substrate. A conducting channel n;cbetween the source and drain can be established by creating an inversion layer of electrons at the semiconductor surface. A field on the order of 1 MV/cm at the silicon surface is necessary to initiate the formation oi this layer. The gate oxide serves as a dielectric spacer allowing this field to be impressed at the silicon/silicon dioxide interface while preventing current flow to the gate contact.

An oscilloscope trace of the electrical characteristics of such a device is shown in Fig. 2 . Also shown in this figure is a circuit diagram defining the measured quantities. The current passing between the source and drain contacts is plotted as a function of the voltage between these contacts. The voltage applied to the gate contact is shown on the right of the figure. The general behavior illustrated in this figure is well understood and the details are discussed elsewhere[3]. We will focus on those features which are pertinent to the role of the gate oxide in the operation of the device. This figure indicates that there is a gate voltage below which there is negligible conduction across the channel. This voltage is called the threshold voltage. It also shows that the current which flows in the channel increases monotonically with the positive voltage applied to the gate. The gate voltages at which the device operates are also worth noting. Operation at voltages below 5 volts is possible only because extremely thin films of high dielectric strength can be reproducibly grown on single crystal silicon. The gate oxide of the device illustrated in Fig. 2 is 25 nm thick.

This figure shows how the current passing between source and drain responds to changes in the field at the Si/SiO_2 interface. Consequently the current flowing in a MOSFET serves as a sensitive detector of charges in the oxide which change the field at this interface. In fact charge has intentionally been introduced into MOSFET gate insulators to form non-volatile memories[5]. On the other hand unintentional charging of the oxide can lead to instabitilies in device operation. Mobile Na^+ ions in the oxide were in the past a severe problem in this regard until sufficiently clean processes and materials were used in manufacture. The interaction of ionizing radiation with the gate oxide also creates instabilities. There are two well-known instances of the latter situation which illustrate the importance of understanding the effects of ionizing radiation on SiO_2.

RADIATION RELATED INSTABILITIES IN MOSFET'S

The first example involves MOSFET's exposed to ionizing radiation in their operating environment[6]. This situation is common in military or satellite applications and the devices must be radiation tolerant. Ionizing radiation in the form of energetic electrons or photons penetrates into the gate oxide region generating electron hole pairs in the oxide. Some of these carriers separate in the presence of the fields impressed on the gate oxide. While about 10% or more of the free holes are captured at traps in the oxide, the majority of electrons pass through without being captured. The accumulation of positive charge lowers the threshold voltage of the device and it fails to operate within its design limits. While radiation can generate traps in the oxide, as we will discuss later, its primary role in this situation is to provide carriers which fill pre-existing hole traps in the oxide. These charges can turn the device on even though no voltage is applied at the gate. The radiation hardness of the device is controlled by empirical processing sequences which minimize the density of hole traps in the completed devices[7,8].

The second instance involves charging of the oxide during the course of normal operation by energetic carriers generated in the semiconductor[9]. High fields are present in the device either across the channel or under it[10]. Mobile carriers entering these regions are accelerated by these fields and are some of these do not come into thermal equilibrium with the silicon lattice. Of these carriers some are energetic enough to surmount the barrier at the silicon/silicon dioxide interface and a small fraction are trapped at defects in the oxide. In the n-channel MOSFET electrons are the mobile carriers and electron trapping instabilities occur. While these instabilities can occur even with the most trap-free oxides, ionizing radiation encountered during processing with electron beams or plasmas creates additional traps in the oxide which aggravate the problem[11,12,13,14]. One example of such a trap is the trapped hole center discussed above. After a hole, produced by radiation, has been trapped on it,this center becomes an efficient electron trap. Other neutral centers generated by ionization of the oxide will be discussed in another section. While these effects do not preclude the use of processes such as electron-beam lithography or reactive-ion etching in the manufacture of MOSFET based circuitry , they do complicate the processing and design considerations. These details have been carefully considered in two recent articles discussing miniature circuits produced using electron beam lithography[15,16].

TRAPPING MEASUREMENTS IN THE MOS SYSTEM

From a scientific point of view, the sensitivity of the MOS system to charges in the oxide makes it an ideal vehicle to study traps in thin SiO_2 films. Physical measurements such as ESR are possible and have been carried out on thin oxide films[17,18,19]. However detection of defects in the film at the part per million level by these techniques requires state-of-the-art sensitivity. An extremely small volume of material is present in films compared to bulk samples. A bulk sample of SiO_2 1 cm^2 in area and 0.5 mm thick contains about 10^{22} atoms. At the ppm defect level there are 10^{16} defects to respond to a particular measurement technique. The theoretical limit for electron spin resonance for example is 5 orders of magnitude below this. On the other hand a thin film sample of the same area 100 nm thick , contains about 10^{17} atoms and 10^{11} defects at the part per million level. ESR measurements on films are therefore more difficult to perform and interpret.

Charge levels an order of magnitude or more below this can be detected with the MOS system. As discussed earlier, this sensitivity results largely from the properties of the underlying silicon. In Fig. 2 a 100 mV change in gate voltage results in an easily measureable change in the drain current of the MOSFET. In this particular example, this voltage change results in a 40 KV/cm change in the field at the silicon surface. Changes of 10mV or less are easily

measureable in these structures. An equivalent change in field results from 10^{10} charges/cm^2 at this interface. The sensitivity can be further increased by careful measurement techniques and device design.

In the case of the MOSFET, the conductivity of the inversion channel in the silicon indicates the field at the Si/SiO_2 interface. In an MOS capacitor the capacitance of the silicon serves to probe this field. Since these structures are easier to fabricate than FET's they are more commonly used in studies of the oxide layer. While the detailed theory of this device is presented elsewhere[20], a brief description is appropriate here. The high-frequency capacitance of an MOS capacitor on a p-type substrate is shown as a function of the applied voltage by the dotted curve in Fig. 3b. The MOS capacitor can be considered as a series combination of two capacitors; an oxide layer whose capacitance is independent of voltage and a semiconducting layer whose capacitance is voltage dependent. A voltage applied to the gate is used to bias the semiconductor. When this semiconductor is forward biased (negative voltage) majority carriers are present in a thin layer at the surface. The semiconductor acts as a metal and the full oxide capacitance is measured. When the semiconductor is reversed biased (positive voltage), majority carriers are driven from the surface forming a depletion layer. This layer has a small but finite capacitance which depends on its thickness and which reduces the total series capacitance of the combination. The flat minimum occurs when the width of the depletion layer stops increasing and reaches a maximum. This behavior depends only on the type and concentration of the dopant in the semiconductor. The capacitance of the system uniquely defines the field at the interface[20].

Both the conductivity of the silicon in the MOSFET structure and its capacitance in the capacitor structure can be exploited to study charges in the oxide. Fig. 3a shows the effect that a sheet of N charges/cm^2 located at position x has on the field in an oxide of thickness t_{ox}. The oxide thickness is measured from the gate to the silicon substrate. The field in the absence of the charge is shown by the dotted line in this figure and is due to the externally applied voltage. As illustrated by the solid line the effect of this charge is to raise the electric field in one region of the oxide and lower it in the other. Since the electric fields at or near the interfaces control the electrical properties of the system, we will focus our discusssion on them. As a consequence of Kirchoff's law, the ratio of the magnitudes of the changes at the interfaces is inversely proportional to their distance from the charged sheet. Using this information along with Gauss' law, the field changes in the oxide can be determined. With the gate as the origin of the coordinate system, the magnitude of the field change at the silicon interface is

$$\Delta E_{Si} = (q/\epsilon) \times N/t_{ox}$$

while that at the gate interface is

$$\Delta E_{Al} = (q/\epsilon)\ (t_{ox}-x)\ N/t_{ox}\ \epsilon$$

where ϵ is the dielectric constant of the oxide and q is an elementary charge. The change in field at the Si/SiO_2 interface changes the capacitance of the capacitor or the conductivity of the FET. This is illustrated for the case of the capacitor in Fig. 3b where the capacitance voltage curve measured with the charge in the oxide (solid line) is shifted from that measured in the uncharged oxide(dotted line). The shift along the voltage axis for both the capacitor or the FET examples is given by

$$\Delta V = (q/\epsilon) \times N$$

Note that this measurement alone can only determine the product of the total charge and its location. The change in field at both interfaces given in the preceeding equations are both required to determine these quantities separately.

The photocurrent excited from both contacts provides the means to probe both of these interfaces and the fields in their vicinity. The use of this technique for centroid determination was developed and discussed by DiMaria[21]. In this measurement energetic photons excite electrons over the barriers at the interfaces. The sign of the field across the oxide and the energy of the incident photons determine the contact from which the electrons flow. The barrier lowering caused by the field near the injecting interface controls the amount of current passing into the oxide. It is this effect which is used to probe the charge distribution in the oxide.

The behavior of the photocurrent with applied voltage in a charge-free oxide is illustrated schematically by the dotted line in Fig. 3c. It should be emphasized that photoelectrons can be excited from the semitransparent gate contact under negative gate bias or from the silicon under positive gate bias. The absolute magnitude of the gate voltage is shown in this figure to denote this behavior. This measurement allows either interface to be probed by simply changing the polarity of the voltage applied to the gate. The effect of the positive sheet charge distribution in the oxide is again illustrated by comparing the dotted (uncharged) and solid (charged) cuves in Fig. 3c. These curves are highly schematic and overly simplified The complications associated with measurements of positive charge by this method are treated extensively elsewhere[22,23]. The voltage shift for injection under positive gate bias(Si injecting) is given by

$$\Delta V_{Si} = (q/\epsilon)\ x\ N$$

This is identical to the shift measured from the capacitance provided that the charge is in the bulk of the sample. For negative gate bias (Al injecting), the shift along the voltage axis is given by

$$\Delta V_{Al} = (q/\epsilon)\ (t_{ox}-x)\ N$$

Note that as x is moved closer to one interface its effect on the field at the other interface diminishes . Correspondingly its effect on the photoinjection from that interface is also reduced. The photocurrent depends on the field in the oxide near the interface. Charge located precisely at an interface has no effect on the the field near either interface; it is compensated exactly by the image charge on that interface and produces no net field change in the oxide.

Two cases are of particular interest to this study. When charge is located in the oxide but much closer to one interface than the other, the photocurrent injected from that interface will be shifted along the voltage axis. The photocurrent injected from the other interface will be relatively unaffected. If the charge is distributed uniformly throughout the oxide, the centroid is in the middle of the film and the field at both interfaces is affected equally. In this case, the photocurrent from both interfaces will be shifted equally along the voltage axis.

Trapping measurements in the MOS system are possible only because charge can be injected into the oxide from the contacts. While other mechanisms such as tunneling can be used the more common techniques are avalanche[24] or photoinjection[25] in capacitors and optically induced hot-electron injection in polysilicon gate MOSFET's[26]. By suitable choice of substrate type and doping concentration either holes or electrons can be injected into the oxide. These injection techniques are posssible only because of the high fields which can be impressed on both the silicon and oxide.

By monitoring the total charge injected into the oxide and the total amount appearing in traps , the capture cross-sections for these traps can also be obtained. The capture cross-sections describe the minimum distance of approach necessary for a carrier to be captured by a trap; it is essentially the area associated with that distance. Experimentally the buildup of charge in the film, as monitored by the shifts in capacitance or source-drain current, is measured as a function of the charge injected per unit area. Assuming that the detrapping is negligible and that first order kinetics are valid, the number of filled traps increases with injected charge in an exponential manner until it reaches a saturation value. The exponential rate of increase is the capture cross-section and the final saturation value is the trap density. By fitting the experimental data to this equation both capture cross-sections and trap densities can be determined. Based on this model the capture cross-section is proportional to the logarithmic derivative of filled trap density with injected charge[24]. Experimentally the only requirement for such a study is that the centroid remain fixed during the injection and that the displacement current is a small portion of the total current in the circuit[11]. In most practical situations the trap density in the oxide is low enough that these criteria are satisfied.

In summary the MOS system lends itself readily to studies of the trap densities, capture cross-sections and locations of hole or electron traps in the oxide. A great variety of traps in SiO_2 have been catalogued and characterized[27]. For the remaining sections of this paper we will deal with those traps which are introduced into the oxide by ionizing radiation.

IONIZING RADIATION EXPERIMENTS: RESULTS AND DISCUSSION

Device fabrication and structure will not be discussed extensively here. These are available on other publications which describe similar experiments in capacitors[11] and FET's[14]. The results presented here are from devices whose gate oxides were grown at 1000° C on <100> silicon substrates. Oxide thickness was between 50 and 25 nm. In the FET's the polysilicon gates were degenately doped with phosphorous and were 350 nm thick. The devices were exposed to ionizing radiation in the form of 25 KV electrons or x-rays. Earlier experiments have shown that traps produced by these two sources are identical[11]. Subsequently electrons or holes generated in the contacts of the devices by the techniques previously mentioned were injected into the gate oxides. These carriers were used to fill the traps present in the oxide. By comparing the trapping before and after irradiation the traps introduced into the oxide by the radiation were studied. Both electron and hole traps in the oxide were studied by separate experiments in which either holes or electrons were injected.

The results of electron beam irradiation on the trapping behavior of polysilicon gate MOSFET's is shown in Fig. 4. In this figure the change in threshold voltage of the device is plotted against the number of electrons injected into the oxide per unit gate area. The threshold voltage change is proportional to the number of traps which are filled as a small fraction of the injected electrons are captured by the traps in the oxide. Devices were irradiated with 25 KV electrons to a total dosage of $10\mu C/cm^2$ and subsequently some of these were annealed for 30 minutes at 400° C in forming gas. The data from these devices are displayed in the two upper curves in this figure. A third sample from the same wafer was not exposed to the electron beam. The lowermost curve in the figure shows the data for this case. Note that the electron beam exposure substantially increases the trapping in the devices and that the anneal has not completely reduced the traps in the oxide to their original level.

Analysis of the two upper curves shows that two types of traps are being filled as electrons are injected. The first kind of trap is positively charged and is completely filled after $5x10^{13}$ electrons/cm^2 have been injected. After this trap has been filled the threshold voltage is returned to normal and the oxide is in a net neutral state. On further injection neutral

centers with lower capture cross-sections begin to capture electrons raising the threshold voltage of the device. Prior to injection the neutral traps are not detectable since they do not change the fields at the interface. Their presence is inferred only by the change in the charge state of the oxide as they capture injected electrons. Recently we have also found that the radiation-induced neutral centers are capable of capturing holes as well as electrons. These results give a significant new insight into the understanding of ionization damage in SiO_2. They show that in addition to supplying carriers to fill traps which pre-exist in the oxide, ionizing radiation also generates new traps in the film. Radiation-induced defects in bulk glasses are generally ascribed to the charging of centers present in the film before irradiation[28]. The incident electrons are not energetic enough to cause displacement damage so that these traps must be associated with electronic processes in the oxide. This will be discussed in more detail in the conclusions.

The electron trapping cross-sections characteristic of these centers is obtainable from an analysis of this figure. As mentioned earlier, the trap cross-sections are proportional to the derivative of the threshold shift with injected charge. The capture cross-section of the positively chared center is about $1x\ 10^{-13}$ cm^2 for the field used in this experiment. The capture cross-section has been shown to be coulombic and field dependent[12,22]. The neutral centers have a continuous spectrum of electron capture cross-sections[11]. These are distributed between 10^{-15} and 10^{-18} cm^2. The cross-section of these centers exhibits a weak dependence on the oxide field[12]. Hole capture cross-sections for traps which pre-exist in the oxide[8] or for traps which are generated by the radiation[29] have also been measured. The capture cross-section for holes in these neutral centers was between $1x10^{-13}$ and $1x10^{-14}$ cm^2. This is probably an overestimate of the actual cross-section[27].

Figure 4 also shows that anneals at 400°C leave residual positive and neutral centers in the oxide underlying the polysilcon gate. While a 400°C anneal removes this charge completely from oxides underlying aluminum gates, anneal temperatures above 550°C are required to remove the charge completely from this polysilicon gate device. The annealing of the positive centers has been shown to depend on the metal present on the gate during the anneal[11]. Aluminum plays an important role in the annealing of this defect which not yet understood. Neutral centers in both aluminum and polysilicon gate devices require temperatures above 550°C to be completely removed.

Another feature which distinguishes the positively charged and neutral traps from each other is their location in the oxide film. In this section it will be shown that the pre-existing centers which are filled by the holes generated by the ionizing radiation are at the interfaces of the film. The neutral centers created by the radiation in an uncharged state are located in the bulk of the oxide. The photemission experiments discussed earlier were used to determine the centroids of these traps in MOS capacitors with semitransparent aluminum gates.

In the case of the positive centers the capacitors were exposed to 25KV x-rays while under positive or negative bias. Photoemission characteristics were taken on the same capacitors before and after the irradiation. The results of these two experiments are shown in Fig. 5 and 6. The photoemission current from the two interfaces is plotted against the voltage across the oxide, obtained by subtracting the silicon surface potential and the contact potential difference from the gate voltage. The high field portion of the emission characteristic is shown to simplify interpretation of the data[22]. After irradiation the characteristics are shifted to lower voltages due to the presence of positive charge in the film. The results under positive irradiation bias are shown in Fig.5. This sample was irradiated and measured twice. The change in flat-band voltage after each irradiation is given in the figure. Under positive irradiation bias only the photocurrent from the silicon is shifted, indicating that the holes are trapped at this interface. The results under negative radiation bias are shown in Fig.6. Under negative irradiation bias only photocurrent from the aluminum is shifted indicating that the

holes are trapped under the gate. These results are consistent with the simple picture of hole transport toward the positively biased interface and electron transport toward the negative one. Electron-hole recombination at the latter interface annihilates any charged centers at this electrode. From the limits of error on these data, the holes are located within 5 nm or less of these interfaces[22]. Similar results are obtained when holes are injected into the oxide using avalanche injection as a source of carriers[29]. In this instance there is no possibility of introducing extra traps into the oxide as there is with radiation.

In the case of neutral centers the capacitors were irradiated with 25KV electrons to a total dosage of $1mC/cm^2$. These electrons are sufficiently energetic to penetrate the oxide layer completely. The capacitors were not biased during the irradiation. After irradiation these aluminum gate capacitors were annealed at 400°C to remove the positive charge from the oxide. Electrons were injected into the oxide to fill the traps. Photoemission characteristics were compared before and after the traps were filled with avalanche injected electrons. Results of this experiment are displayed in Fig. 7. After injection the characteristics are shifted to higher voltages consistent with the presence of negative charge in the film. Note that the shifts for injection from the silicon are approximately equal to those from the gate. This places the centroid in the middle of the oxide since the charge has essentially the same effect on either interface. This result implies that the electrons trapped in the neutral centers are distributed uniformly throughout the oxide. Experiments in which holes are avalanche injected into the oxide layer of MOS capacitors have been recently performed in our laboratory. Although the data interpretation is quite complicated, the results are consistent with those presented above for electron trapping. After irradiation additional hole traps are found in the bulk of the oxide[29].

The results in Fig.7 show that radiation introduces additional traps which may trap holes or electrons. As the results in Fig.5 and 6 demonstrate, no evidence has been found that these new traps are charged with either carrier after irradiation. Since equal numbers of holes and electrons are produced by the radiation recombination is a likely event. For this reason the trapped holes accumulate at the interfaces where the fields make recombination with electrons less probable. Holes or electrons trapped in the bulk of the oxide would result in large local fields which enhance the probability of recombination. When both carriers are present, holes trapped in the bulk would tend to recombine with electrons. On the other hand, avalanche or photoinjection is a single carrier injection process where little if any recombination takes place. Under these injection conditions, it is possible to charge the traps once they have been created by the radiation.

The number of these traps depends on the total dosage to which the oxide was exposed. The dosage dependence of trap generation is illustrated in Fig. 8. In this figure the number of trapped holes and neutral traps measured in polysilicon gate MOSFET's is plotted against the number of incident 25 KV electrons which produce the damage. In these experiments electrons were injected into the oxide to determine the trap densities. While the total number of positive centers is shown on this figure , only the neutral traps with electron capture cross-sections above 10^{-16} cm^2 are measured. The background density of positive charge in unirradiated samples is below $10^{10}/cm^2$. The background density of neutral centers is coincident with the trap density measured at the lowest dosages.

The dosages used to irradiate the samples are relatively high but can be encountered during device processing[15,30]. For example at this energy a dosage of $10\mu C/cm^2$ results in about 10 Mrads(Si) being absorbed in the oxide. Dosages at this level are necessary to produce color centers in crystalline or vitreous SiO_2 in bulk form[28]. The density of both positive and neutral centers increases quite slowly with increasing dosage. However the positive charge shows an initial buildup at dosages two orders of magnitude lower than the neutral centers. Color center formation in bulk SiO_2 also shows the same slow buildup and

two stages of growth[28]. The saturation of the positive charge at high dosages is a consequence of the buildup of a retarding field at the interfaces which prevents further buildup of charge in these regions[6]. In this particular case the sample was not biased and the charge buildup saturated when it equalled the internal field due to the work function difference between the gate and substrate. The total number of hole traps at the interfaceis higher than that shown here. The neutral traps on the other hand continue to increase slowly after saturation of the positive centers. The same slow increase is noted when holes are used to probe the bulk neutral centers which are created by the radiation.

These results independently affirm that different mechanisms are responsible for the formation of the centers. While additional hole or electron traps may be formed in the bulk at high dosages, electron-hole recombination in the bulk prevents these centers from obtaining a net charge during the irradiation. For this reason the positive charge measured in this experiment is mainly determined by the filling of pre-existing hole traps in the oxide. The *neutral centers do not exist prior to the irradiation and are generated during the irradiation.* The formation mechanism for the neutral centers in SiO_2 is not clear at this time. However ionizing radiation is known to create new defects in the alkali halides[32]. In this material strictly electronic processes, involving electron-lattice interactions are thought to produce these centers[33]. These processes require multiple events and are inherently lower probability events than charge capture by an existing defect. This may explain why neutral center formation requires higher dosages than the positive center. Neutral center formation which involves the actual creation of a new trap is expected to require higher dosages than the trapping of a hole, generated by the radiation, at a pre-existing center. This dosage dependence of the neutral centers is consistent with the production of traps by random interaction of the radiation with centers in the oxide. These centers have some probability for conversion to a trap when they interact with radiation. Those centers with the highest conversion probability are converted at the lowest dosages and soon saturated. Additonal centers with lower conversion probabilities are the next to be converted . A continuous spectrum of these centers would account for the shape of this curve.

CONCLUSIONS

The effects of ionizing radiation on thin SiO_2 films have been examined and their technical importance has been described. The electrical properties of the MOS system have been shown to be an ideal vehicle for studying them and the results of such studies have been presented. In addition to filling pre-existing hole traps at the oxide interfaces, it has been It has been demonstrated that ionizing radiation creates additional traps in the bulk of the oxide, in addition to supplying carriers to pre-existing traps at the interfaces. These traps have no net charge immediately following irradiation but can trap either electrons or holes which are injected subsequent to irradiation. While hole traps are filled at relatively low dosages, higher dosages are required to create the neutral centers.

Models describing the positive centers on an atomic level have been discussed by Mott and Griscom at this conference and previously by others[34,35]. The E_1' center in particular has been identified with this charged defect[36]. The neutral center has not previously been observed and its atomic nature is not well understood. Its general properties allow some conclusions to be drawn. The trap is probably dipolar in nature. Such a center would appear to be neutral at a few atomic diameters from its location and still be capable of capturing electrons or holes which approach within a critical distance. The capture cross-sections observed for the neutral centers are consistent with this picture[11]. While the hole and electron traps discussed here may not necessarily occur on the exact same defect, such a situation is plausible in this model. The negative side of the dipole can trap holes and the positive side trap electrons. Such a center could be formed when ionizing radiation breaks a bond in the SiO_2 . Some time would elapse before the bond could be re-established. If during this time a

slight lattice relaxation occurs, this bond would not be reformed in its original configuration. Such a configuration results in positive and negative charges separated by a short distance; a dipolar center. Based on the capture cross section data these distances are less than a few hundredths of a nanometer[11].

No evidence is available at this time to determine if these centers are formed from impurities in the SiO_2 or from intrinsic centers. ESR and optical studies of bulk or thin film samples would lend some insight in this regard. Integrating this center into the list of defects already identified in bulk glasses is an interesting challenge.

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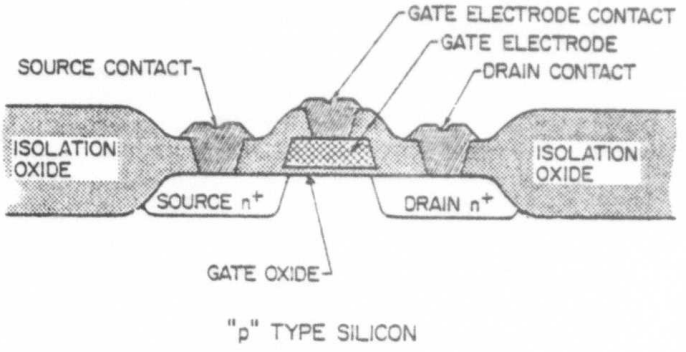

Fig.1 Schematic cross-section of an n-channel enhancement mode MOSFET. The figure shows the use of SiO_2 to isolate the active device from other active devices and to couple the voltage applied at the gate to the underlying p-type semiconductor. This voltage is used to control the current passing between source and drain.

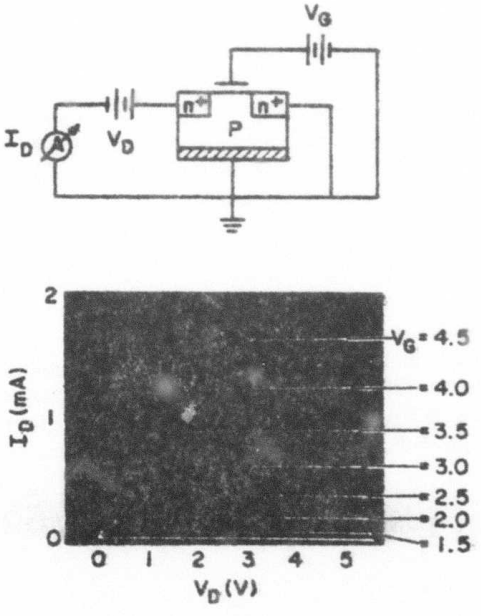

Fig.2 The effect of gate voltage on the current between source and drain is illustrated in this figure. The source-drain current is plotted against the voltage between these contacts. A circuit diagram defining the measured quantities is also given. The gate oxide of this device is 25 nm thick.

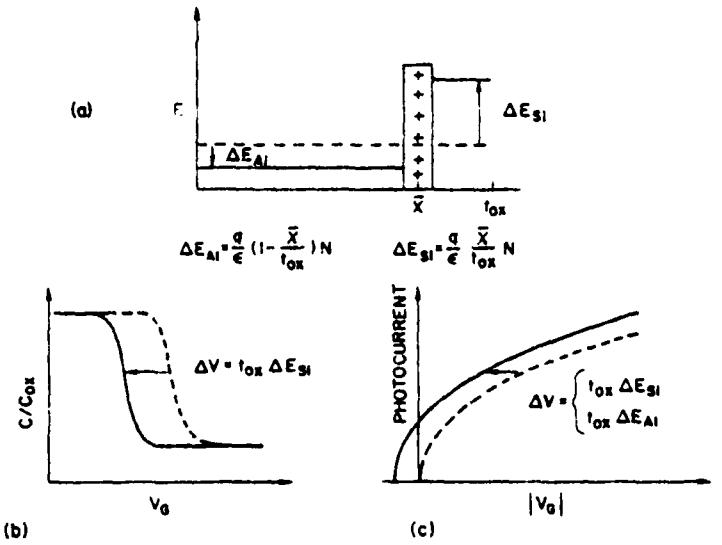

Fig.3 The effect of a positive charge sheet on the interface fields (Fig. 3a), high frequency capacitance (Fig.3b), and photoemission current (Fig.3c) of an MOS capacitor. The *dotted lines denote these quantities when* the oxide is free of charges and the solid lines show how N charges per unit area, located at a position x in the film change their behavior. The changes in the interfacial fields are also given in Fig. 4a. The oxide is assumed to have thickness t_{ox} and dielectric constant ϵ.

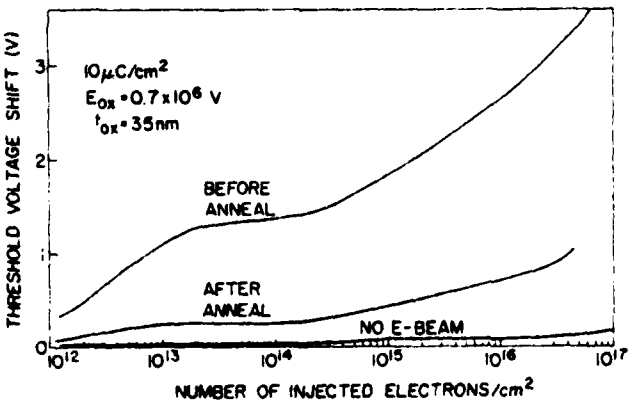

Fig.4 The threshold voltage shift which occurs as injected electrons are trapped at defects in the gate oxide is plotted against the number of electrons which have been injected into the oxide per unit gate area. These measurements were made on polysilicon gate MOSFET's whose gate oxide was 35 nm thick. A field of 0.7 MV/cm was present across the oxide during the injection.

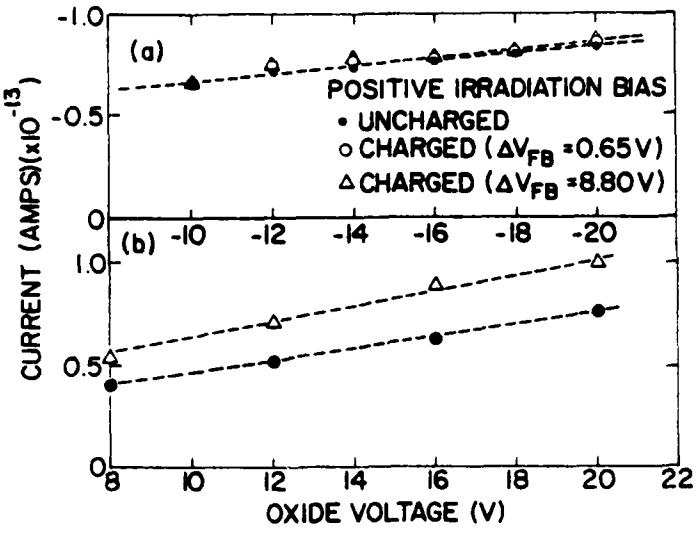

Fig5. The photoemission characteristics of an MOS capacitor with a semitransparent aluminum gate are shown before and after irradiation under positive bias. These samples had 50 nm oxides which were subjected 25KV X-rays. The capacitor was irradiated and measured twice as shown in the figure. In this case the charge is located at the Si/SiO_2 interface.

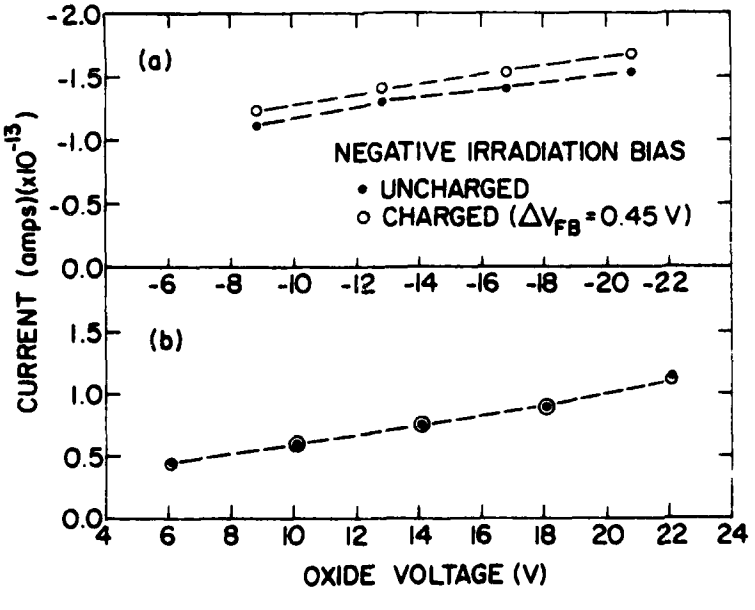

Fig.6 The photoemission characteristics of an MOS capacitor with semitransparent aluminum gates are shown before and after irradiation under negative bias. Except for the sign of the bias all the experimental conditions are similar to those described for Fig.5. In this case, the data indicates that the charge is located at the Al/SiO_2 interface.

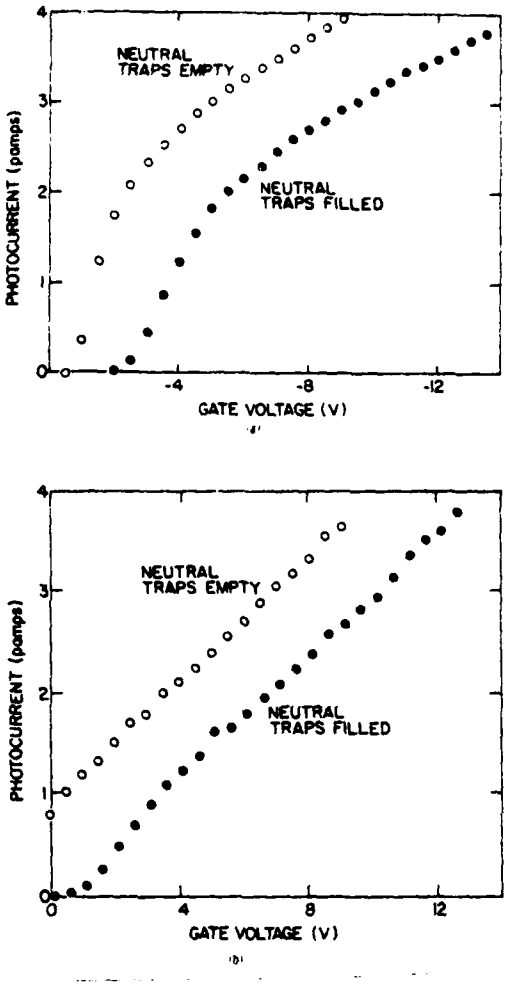

Fig.7 The photoemission characteristics of an MOS capacitor with a semitransparent aluminum gate are shown before and after the neutral centers created by irradiation are filled with electrons. The photocurrent measured from the aluminum interface is shown in Fig.7a while that from the silicon is shown in Fig.7b. These capacitors had 50 nm thick oxides and were irradiated with 25KV electrons. These results indicate that the neutral centers are distributed uniformly throughout the oxide.

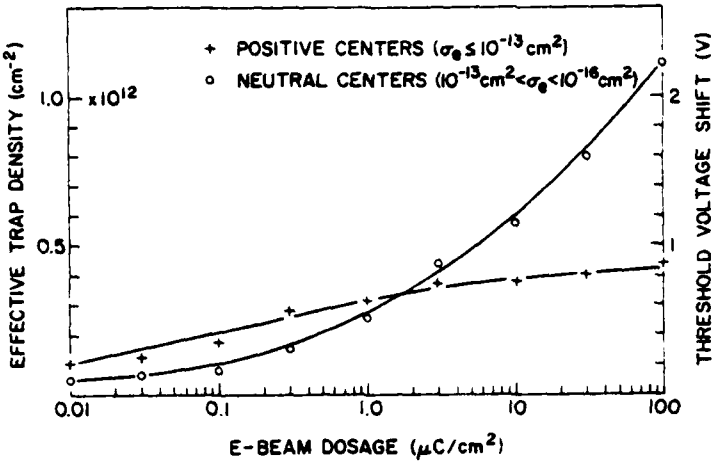

Fig.8 The density of positive and neutral centers present in the gate oxide of a polysilicon gate MOSFET is plotted against the total number of 25KV electrons incident per unit surface area. While the total number of positive centers is shown in this figure, only the neutral centers with cross-sections less than 10^{-16} cm^2 are shown. The gate oxide in this device is 45 nm thick.

ATTENUATED TOTAL REFLECTANCE STUDY OF SILICON RICH SILICON DIOXIDE FILMS

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ABSTRACT

The infrared absorption of Si rich SiO_2 films has been measured using the attenuated total reflection technique. Absorption lines attributed to SiOH, H_2O and SiH groups have been observed in the as-deposited films. The concentrations of these impurities were found to be in the mid 10^{18} cm^{-3} range. Following a 1000 C anneal no absorption lines were observed, and the concentration limit was found to be less than the mid 10^{16} cm^{-3} range.

Currently, there is much interest in silicon rich silicon dioxide films (commonly called semi-insulating polycrystalline silicon, SIPOS) for passivation[1,2] and non-volatile memory device[3,4] applications. Previous investigations using Auger electron spectroscopy (AES), X-ray diffraction, transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS) have shown the presence of elemental silicon and various silicon oxide phases in these films[5,6]. In a recent study, Hartstein et. al.[7] have shown that the as-deposited Si rich SiO_2 films consist of regions of amorphous silicon within an SiO_2 matrix, and subsequent annealing above 1000 C crystallizes the amorphous regions. The size of these crystalline regions had been previously shown to be $\leq$ 100 Å, increasing with annealing temperature and only weakly dependent on oxygen concentration[5].

Pliskin[8] has investigated the infrared absorption properties of thick SiO_2 films deposited in a variety of ways. Of particular interest to us, he has quantified the infrared absorptions due to SiOH and H_2O groups in these films. Beckmann et. al.[9] and Murau et. al.[10] have used the attenuated total reflection (ATR) technique to look at the infrared absorption due to SiOH, H_2O, and SiH groups in thin (< 1000 Å) SiO_2 films. In this paper we present the results of an attenuated total reflectance study of Si rich SiO_2 films. We find significant amounts of SiOH, H_2O, and SiH groups in the as-deposited films, but no detectable impurities following a 1000 C anneal.

For this study, both SiO_2 and Si rich SiO_2 films were chemically vapor deposited (CVD) at 700 C on silicon total internal reflection elements to a thickness of 1000 Å. Using techniques previously described[11], the CVD Si rich SiO_2 films were fabricated using a ratio, R_0, of the concentration of N_2O to SiH_4 in the gas phase equal to 3, and contained 46 atomic percent Si. After measurement, the samples were cleaned in alkali and acid peroxide solutions using a procedure similar to that used by Irene[12], but without HF, and subsequently annealed at 1000 C in N_2 for 30 min.

The infrared spectra were obtained using a Perkin Elmer Model 180 spectrometer. The internal angle of incidence in the silicon total internal reflection element was 32°, and the geometry was such that 80 internal reflections were obtained. The spectra obtained for the CVD SiO_2 film both as-deposited and following the 1000 C anneal are shown in Fig. 1. The corresponding spectra obtained for the CVD deposited Si rich SiO_2 film both as-deposited and following the 1000 C anneal are shown in Fig. 2. Both of the as-deposited films exhibit absorption lines at 3640 cm^{-1}, 3400 cm^{-1}, and 2260 cm^{-1}, which are absent after annealing. The lines at 3640 cm^{-1} and 3400 cm^{-1} have been attributed to SiOH and H_2O groups, respectively.[8] The line at 2260 cm^{-1} has been attributed to the SiH group.[9,10] It is clear from the spectra that more impurities are present in the Si rich film than in the pure SiO_2 film, particularly the SiH group. It is also clear that annealing at 1000 C removes these impurities from the films. In what follows we seek to determine the actual concentration of impurities represented by the absorption lines in the spectra.

Pliskin[8] has analysed the silanol (SiOH) and water content of SiO_2 films gravimetrically and related the weight percents to the strengths of the infrared absorptions. The relationships given are

$$W = (-14A_{3650} + 89A_{3330})(2.2/\rho) \quad \text{and} \tag{1}$$

$$S = (179A_{3650} - 41A_{3330})(2.2/\rho), \tag{2}$$

where W is the wt. % water (including H_2O from "easily" removed silanol), S is the wt. % OH as silanol, ρ is the density of the film in g/cm^3, and A_ν is the optical density per μm of film at frequency ν. In the analysis that follows, we take the density of the films to be 2.2 g/cm^3, and identify our 3640 cm^{-1} absorption with Pliskin's 3650 cm^{-1} absorption, and our 3400 cm^{-1} absorption with his 3330 cm^{-1} absorption. The weight percentage determination is easily changed to a concentration determination by using the atomic weights of the species involved.

In order to utilize Eqs. 1 and 2 to determine the concentration of silanol and water in the SiO_2 films, we must calibrate the absorption strength measured in our particular ATR geometry. We have chosen a direct method of accomplishing this. The absorption band in transmission of SiO_2 near 1600 cm^{-1} was accurately measured using a 6.56 μm thick sample annealed at 1000 C. The strength of this absorption was then compared to the same line measured on the annealed samples using the ATR geometry. From this comparison it is found that the effective gain from this ATR geometry was a factor of 92 over a transmission measurement. Using this factor and Eqs. 1 and 2, the concentration of SiOH and H_2O groups in the SiO_2 films can be calculated. The results of this calculation are shown in Table 1. The entry for the annealed films gives the upper limit of the concentration of these impurities that can be set from the present measurement. It does not represent the limits of the sensitivity of the ATR technique.

The correlation of the infrared absorption of the Si-H bond to concentration has been worked out in detail by Brodsky et. al.[13] They give the following relation for the concentration of any species to its absorption.

$$N = \frac{(1+2\epsilon_m)^2}{9\epsilon_m^2} \frac{N_A n}{(\Gamma/\zeta)} \int \frac{\alpha(\omega)}{\omega} d\omega \qquad (3)$$

where N is the concentration of Si-H bonds, $\epsilon_m = 2.2$ is the optical dielectric constant of SiO_2, N_A is Avogadro's number, n is the number of host bonds in units of m-mole/cm^3, Γ is the absorption strength of the Si-H bond in units of cm^2/m-mole, ζ is the number of Si-H bonds per silicon atom (taken to be 1 for our case), α is the absorption coefficient and ω is the frequency. Following Brodsky et. al.[13], we take $\Gamma = 3.5$ for Si-H bonds. Brodsky's[14] nuclear analysis of the H content of amorphous silicon films shows that Eq. 3 overestimates the Si-H concentration by a factor of 2.

In order to calibrate the determination of the concentration of Si-H bonds, we have used a technique similar to that described above. Using the transmission data of the thick SiO_2 film

and Eq. 3, we have obtained the value of $\Gamma = 0.094$ cm^2/m-mole for the particular vibrational mode of SiO_2 giving the 1600 cm^{-1} absorption. Using this value and the absorption data for the same line in the ATR spectrum, it is possible to calibrate the integrated absorption lines in a similar way to the procedure already used to calibrate the absorption intensities. With this scaling procedure, the absorption lines at 2260 cm^{-1} were analysed using Eq. 3, including the factor of 2 correction, in order to obtain the concentration of Si-H bonds in the samples. These results are also given in Table 1.

From these results it is clear that the amounts of silanol and water in both the as-deposited Si rich SiO_2 and the CVD SiO_2 films are comparable. The Si rich film shows somewhat more silanol and almost a factor of 2 more water than the normal CVD film. The Si rich film also shows more than 10 times more SiH than the normal CVD film. This fact is consistent with the presence of excess Si, but the concentration of SiH does not even come close to accounting for the majority of excess Si present in the film. The excess Si is predominantly contained in seggregated amorphous silicon regions.

It is also important to note that the frequency of the SiH absorption observed (2260 cm^{-1}) is not the same as observed for SiH bonds in amorphous Si,[13] but is rather close to the Si-H bond (2280^{-1}) found in amorphous SiO_2.[15] Therefore, although it might be tempting to suppose that the hydrogen is present in the amorphous Si regions, that appears not to be the case. It must be present in the SiO_2 itself (it is also observed in the normal CVD SiO_2) and possibly also at the interfaces between the SiO_2 and the amorphous Si regions.

There is an additional small absorption line at 2140 cm^{-1} which we have been neglecting up till now. It is close to the absorption line expected for Si-H bonds in amorphous silicon when either O of N is present in the back bonds of the Si.[15] If this identification is correct, the absorption corresponds to a uniform density of 3.8×10^{17} cm^{-3}. Equivalently, it corresponds to a hydrogen density in the amorphous silicon regions of 3.1×10^{18} cm^{-3}. It should be noted that this absorption line is only seen in the Si rich films.

It is quite difficult to assess the possible error present in the concentrations determined using this procedure. In the ATR work of Beckmann et. al.[9], they claim an accuracy of only an order of magnitude. The present experiment is much better than that since we used a direct experimental method of calibrating the ATR method rather than the theoretical calculation used by Beckmann et. al.[9] The absolute accuracy is then probably better than a factor of 2, and the relative accuracies of the concentrations considerably better than that.

In passing, it is worth noting that in the Si rich SiO_2 film, one additional absorption line can be detected which is not present in either the CVD oxide or the annealed samples. The line appears at 1770 cm^{-1}. We have not identified the mechanism responsible for this absorption as yet. It could be due either to bonding differences in the Si rich oxide or to an additional impurity.

In conclusion, we have measured the infrared absorption of Si rich SiO_2 films using the attenuated total reflection technique. The films were found to contain substantial amounts of SiOH, H_2O and SiH groups. These impurities were found to disappear following a 1000 C anneal.

We wish to thank M. H. Brodsky for many helpful discussions as well as a critical reading of this manuscript.

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TABLE 1

	Impurity Concentration (cm^{-3})		
	SiOH	H_2O	SiH
Si rich SiO_2 as-deposited	5.2×10^{18}	3.9×10^{18}	1.0×10^{18}
CVD SiO_2 as-deposited	4.0×10^{18}	2.3×10^{18}	8.5×10^{16}
Si rich and CVD SiO_2 1000 C anneal	$< 5 \times 10^{16}$	$< 3 \times 10^{16}$	$< 1 \times 10^{16}$

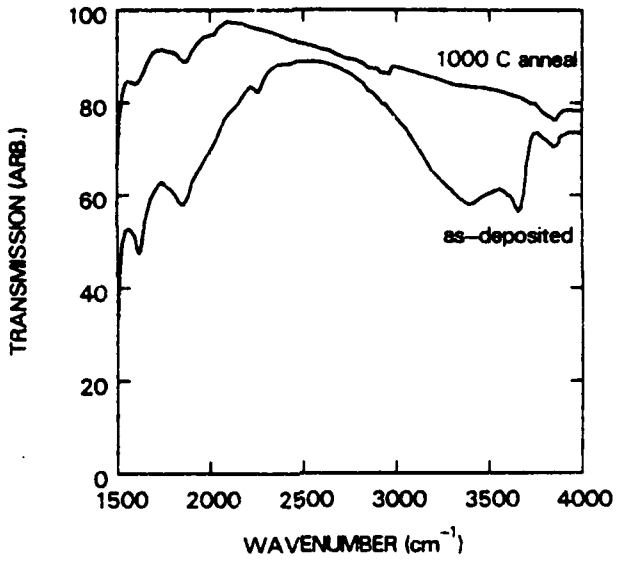

Figure 1 shows the infrared ATR spectra for CVD deposited SiO_2 films both as-deposited and following a 1000 C anneal. Because of the ATR geometry, the units of transmission should be regarded arbitrary. The curve for the 1000 C anneal has been shifted upward for clarity. Prior to this shift the transmissions at 4000 cm^{-1} were equal.

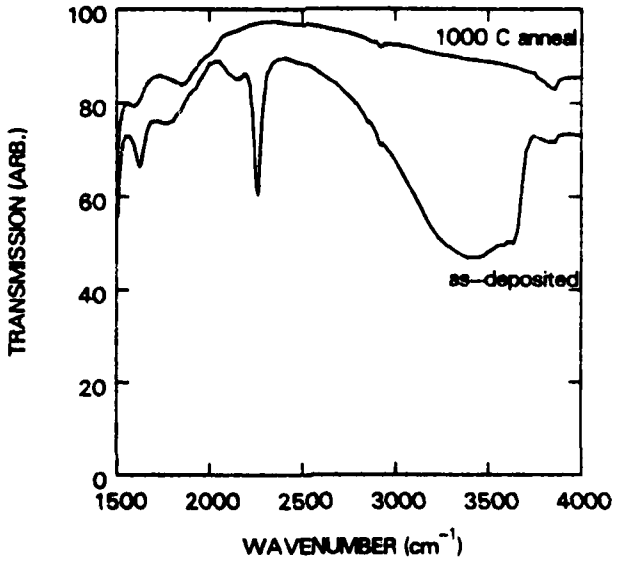

Figure 2 shows the infrared ATR spectra for CVD deposited Si rich SiO_2 films both as-deposited and following a 1000 C anneal. The transmission is in arbitrary units, and the 1000 C anneal curve has been shifted for clarity. Prior to this shift the transmissions were equal at 4000 cm^{-1}.

Reduction of Electron Trapping in Silicon Dioxide by High Temperature Nitrogen Anneal*

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Abstract:

Electron trapping in silicon dioxide is reduced by nitrogen annealing in a furnace system with very low moisture content and special cooling techniques. The flatband voltage shift resulting from injected hot electrons is significantly reduced by the annealing together with the interface states generated. The trapped charge is laterally nonuniform when the oxide is not annealed. From photo I-V measurements, the density of electrons trapped in the bulk of the oxide is reduced by this treatment. The distribution of the trapped charge changes from a uniform distribution in the bulk for a one hour anneal to a distorted U shape distribution, with a larger build-up on the aluminum-silicon dioxide side for a 17 hour anneal. The density of trapped charge close to the silicon-silicon dioxide interface is reduced and thus the small flatband voltage shift. With the reduction in bulk charge, interface state charge becomes important.

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Electron trapping in silicon dioxide is a problem in the long term stability of MOSFETs [1] and an important degradation mechanism in EAROMs [2]. Reduction of electron trapping is thus very important for integrated circuit technology. This paper describes techniques to significantly reduce the effect of electron trapping in a metal-oxide-silicon system. Electron traps in silicon dioxide can be divided into two groups by their different origins. The first group consists of traps that are introduced after the oxide is grown: radiation induced traps [3] and traps from implantation [4]. The second group of traps are the ones that are present in as-grown oxide [5,6]. These as-grown oxide traps have recently been studied and are found to be distributed uniformly in the bulk at room temperature [6]. They are believed to be related to water centers [7] and annealing of the oxides for extended periods reduces the density of these traps [5,6]. The exact effect of the annealing is, however, not understood. In the present work, we have repeated the annealing experiments and discovered that by very carefully excluding moisture from the oxidation system, oxides with very low density of bulk traps can be obtained. The results of the annealing experiment and the trapping properties of such oxides are reported in this paper.

The furnace system for oxidation and annealing has been described previously [8]. The important features are a double-walled quartz tube with dry nitrogen flowing between the walls, and the preburning and cold trapping of the gases to reduce the amount of moisture to less than 1 ppm. The system is kept dry for a few days before oxidation and annealing as it takes a long time to reach the driest level. Another important step is to remove the wafers into a chamber flushed by dry nitrogen continuously at room temperature, instead of exposing them to the atmosphere while they are hot. Failure to cool the samples in a dry environment will give a high density of traps even after the long time anneal. It is postulated that the oxide at high temperature will absorb moisture very easily. For the present experiment, 500 Å of oxide is grown at 1000°C and annealed in nitrogen at the same temperature for different times. The wafers are metallized right after annealing. Aluminum 135 Å thick is evaporated onto the oxide through metal masks to give 32 mil diameter capacitors. The thin transparent aluminum electrode is necessary for photo I-V measurements [9]. The wafers are then annealed in forming gas at 400°C for 20 minutes. The system for avalanche and flatband tracking has been described previously [6]. High frequency and quasistatic capacitance and photo I-V curves [9] are measured before and after injection to determine trap distribution and charge density.

Figure 1 shows the flatband voltage shift as a function of injected charge for three 500 Å oxides annealed for 0, 1, and 17 hours, respectively. The injection is carried out at 100°C to minimize the effect of positive charge [6]. It can be seen that the flatband voltage

shifts are significantly reduced by annealing. The total shift is much smaller than what was reported previously [5,6]. The effective trapped charge per unit area (ΔN_{eff} in [5]) is only $8 \times 10^{10}/cm^2$ for the 17 hour oxide after the injection of $10^{18}/cm^2$ electrons. This is to be compared to the best values of $1.7 \times 10^{12}/cm^2$ in [5] and $2.5 \times 10^{11}/cm^2$ in [6]. Figure II, III and IV show the capacitance curves before and after injection of $10^{18}/cm^2$ electrons for the three oxides. The shift in high frequency capacitance is much smaller for the 17 hour oxide. More importantly, there is also less interface state generation, which can be seen from the smaller distortion in the high frequency curve and the steeper dip in the quasistatic curve. For the oxide that is not annealed, there is evidence that the charge trapped in the oxide is laterally nonuniform. Part of the capacitance distortion comes from real interface states and part of it comes from nonuniformity. Since it is difficult to separate the two components, an apparent interface state density is calculated from the quasistatic and high frequency capacitance curves as a measure of the effect of hot electron injection. This large lateral nonuniformity of the trapped charge has not been observed before in other trapping experiments. The important difference in the present case is that the wafer was pulled from the furnace with oxygen flowing. A 5 minute nitrogen anneal is sufficient to remove the large nonuniformity. The detail of the process is now being investigated. For the oxides that are annealed, the amount of lateral nonuniformity is very small and the calculated interface density states is real. Interface states introduce additional charge in the oxide silicon system and the flatband voltage may not be the best point for measuring charge in the oxide [10]. One important feature of the interface state spectrum, shown in Fig. V, is the increase in interface state density above midgap towards the conduction band. The increase may be exaggerated by lateral nonuniformity but is definitely a real effect. This is similar to the interface state spectrum observed in radiation damaged oxide [11] and the two processes may be related. This may also explain the larger shift of the quasistatic curve on the inversion side compared to the flatband side seen most clearly on Fig. IV. If the interface states above midgap are acceptors [10], they will be negatively charged when the Fermi level moves above the states, which is the case when the surface is inverted. This has a very important consequence. As the threshold voltage of n-channel MOSFETs is determined by the onset of inversion, the threshold voltage shift will be larger than the flatband voltage shift measured in capacitors. Both bulk electron charge and interface state charge contribute to the shift of the threshold voltage. When the bulk charge is lowered, the interface state charge becomes important.

The photo I-V curves for positive and negative biases are shown in Fig. VI, VII and VIII. The interpretation of photo I-V curves is complicated in the present case because of interface effects. When the charge is located in the bulk of the oxide, the photo I-V curves

will be shifted in a parallel fashion down to the zero current level [9]. When the charge density changes close to the interface, the photo I-V shift will no longer be parallel, but converges or diverges, depending on whether the charge is positive or negative. When there are both positive and negative charges, the shift is determined by the net charge. This is the basis of the technique developed by Powell and Berglund [12] to profile the charge. However, when there is charge that is very close to the interface, the discreteness of the charge may give a laterally nonuniform field at the interface even though the charge distribution is laterally uniform and the measured photocurrent will be higher than if the field is uniform. For photo I-V shifts that are diverging, as is the case in the 17 hour oxide [Fig. VIII], the divergence cannot be explained by nonuniformity in the electric field. If nonuniformity is a problem, the real curve should diverge even more. The present result shows that there is a net build up of negative charge towards the interface and the voltage shift at the highest field can be a measure of the lower limit of the amount of net negative charge in the oxide that is contributing to changing the electric field at the injecting interface. For the 1 hour oxide [Fig. VII], the photo I-V shifts are parallel down to almost the zero current level. This means that the charge is distributed in the bulk with little or no build up towards the interfaces. The shifts for the unannealed oxide [Fig. VI] are different from the others. The curves are parallel in the high field region but are divergent in the low field region. This is due to the laterally nonuniform charge distribution. Different regions with different density of trapped charge will give different photo I-V shifts. The final curve is the sum of contribution from the different regions. The curves become parallel when all the regions are contributing to the shift. The parallel voltage shift is a measure of the average charge density in the oxide and will be used accordingly. It must also be noted that the accuracy of the photo I-V measurement is limited when the shifts are very small or when the slope of the curve is very shallow.

Using the above interpretation, one obtains a total charge density of $4.3 \times 10^{12}/cm^2$ for the unannealed oxide, $1.2 \times 10^{12}/cm^2$ for the 1 hour oxide and $1 \times 10^{12}/cm^2$ for 17 hour oxide. These are typical numbers and they may vary by $\pm 25\%$ from capacitor to capacitor. There is a large drop of total oxide charge with the 1 hour anneal but only a small additional drop for the 17 hour anneal. The distribution is, however, very different. For the unannealed oxide, the charge is distributed in the bulk and laterally nonuniform. Looking at the average charge density, the charge centroid is in the center of the oxide. The charge in the 1 hour oxide is approximately distributed uniformly in the bulk with a charge centroid again in the middle of the oxide. For the 17 hour oxide, there is build up of charge towards the two interfaces and a lower density of bulk traps. In fact, a larger fraction of the charge is located near the aluminum-silicon dioxide interface. Since the effect of the charge on the band

bending in silicon is weighed by the inverse of the distance from silicon, the effect of the trapped charge on the silicon is significantly reduced. It must be noted that there is a discrepancy between the maximum positive photo I-V shift and the midgap voltage shift measured by capacitance. The photo I-V shift is larger indicating a compensating positive charge at the interface [6]. The density of the positive charge is also reduced by annealing.

The origin of this change in distribution is still being investigated. The injection of hot electrons and the subsequent trapping at different sites is a technique to locate trap centers in the oxide. Using suitable approximations, the capture cross section and density of different traps can be calculated by studying the kinetics of the trapping process [6]. However, the physical origin of the traps cannot be determined by this experiment alone. Traps from different sources may have the same electrical cross section and would not be separated in the trapping study. In order to identify the physical origin of the traps, other control or analytical experiments must be performed to correlate the results. In fact, the trap centers may be generated by the avalanche and hot electron injection, especially at the interface. It was postulated that the traps in as-grown oxide are due to water related centers. The fact that bulk traps are reduced by annealing is consistent with this explanation, but it is by no means the only explanation. The build-up of traps at the interfaces may come from the redistribution of water related centers or the appearance of other trap centers due to annealing. Recent infrared experiments [13] have shown that during annealing, the Si-OH bond in silicon dioxide is converted into H_2O which is then redistributed. The redistribution may be responsible for the observed charge profile. The exact process is now being studied. As the oxide is being annealed, it is possible that defect centers and impurities are localized near the two interfaces. They may act at trap centers directly or they may enhance diffusion of silicon at the silicon-silicon dioxide interface and diffusion of aluminum when the metal is being deposited at the aluminum-silicon dioxide interface. Both may give rise to trap centers. Another possibility is a nitrogen reaction at the interface [14] which may provide new trapping sites. In fact, a higher initial interface state density and fixed charge are measured for the 17 hour oxide [15]. This may explain the charge build-up in the silicon – silicon dioxide interface. Experiments are now being planned for annealing in argon instead of nitrogen to answer this question.

In conclusion, we have shown the effect of high temperature annealing in reducing flatband voltage shift and interface state generation after avalanche injection. The effect is dramatic if special precautions are used. The annealing reduces and also changes the distribution of traps in the bulk of the oxide. Understanding of the process is important in the optimization of processing for reducing trapping. Further experiments are now in progress for more detailed studies of this and other related effects.

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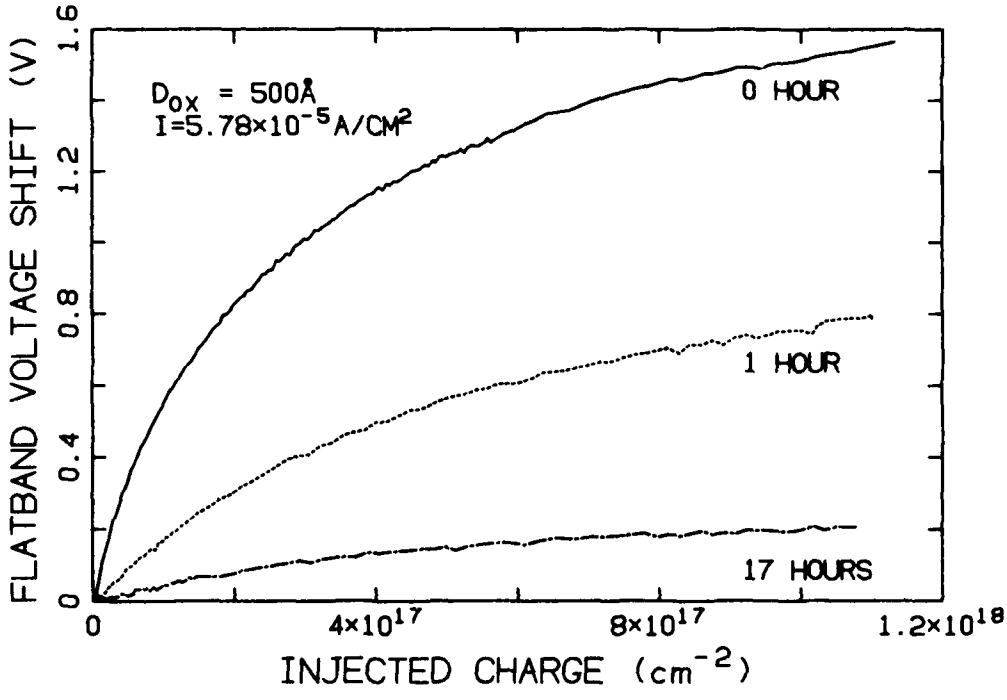

Fig. I Flatband voltage shift as a function of injected charge for 500 Å oxides that are annealed in nitrogen for 0 hour, 1 hour and 17 hours, respectively. Injection was carried out at 100°C.

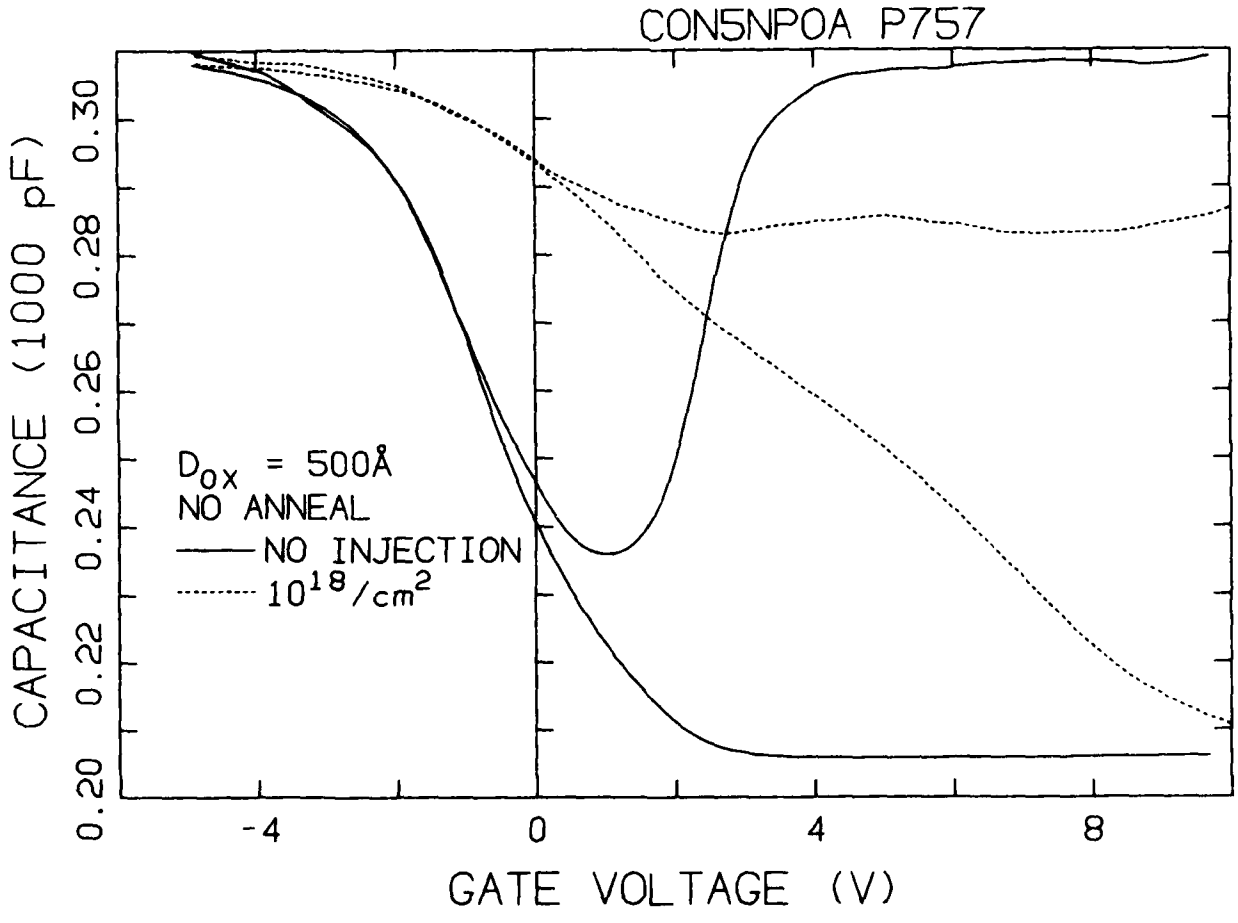

Fig. II High frequency and quasistatic capacitance before and after injection of $10^{18}/cm^2$ electrons for an oxide that has not been annealed in nitrogen.

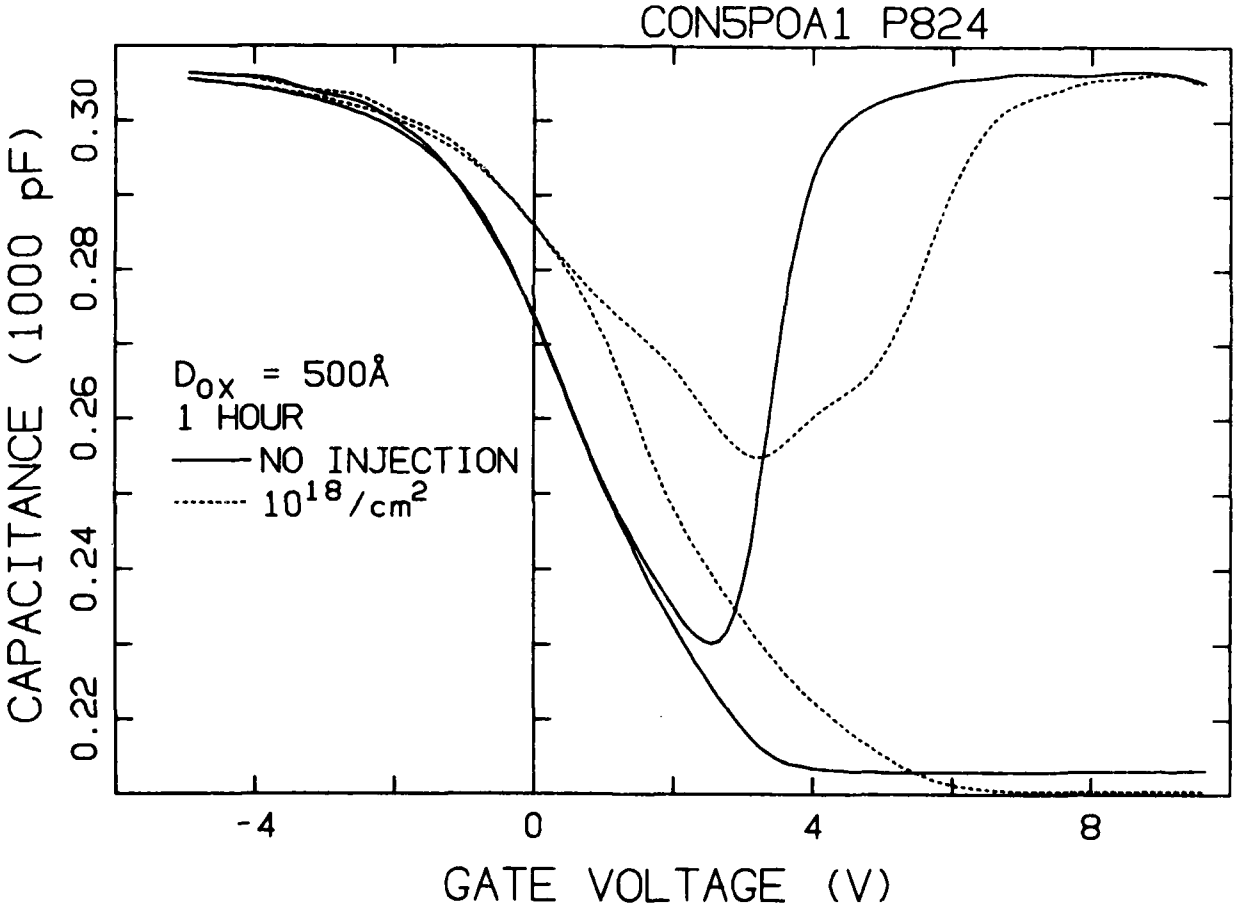

Fig. III High frequency and quasistatic capacitance before and after injection of $10^{18}/cm^2$ electrons for an oxide that was annealed in nitrogen for 1 hour.

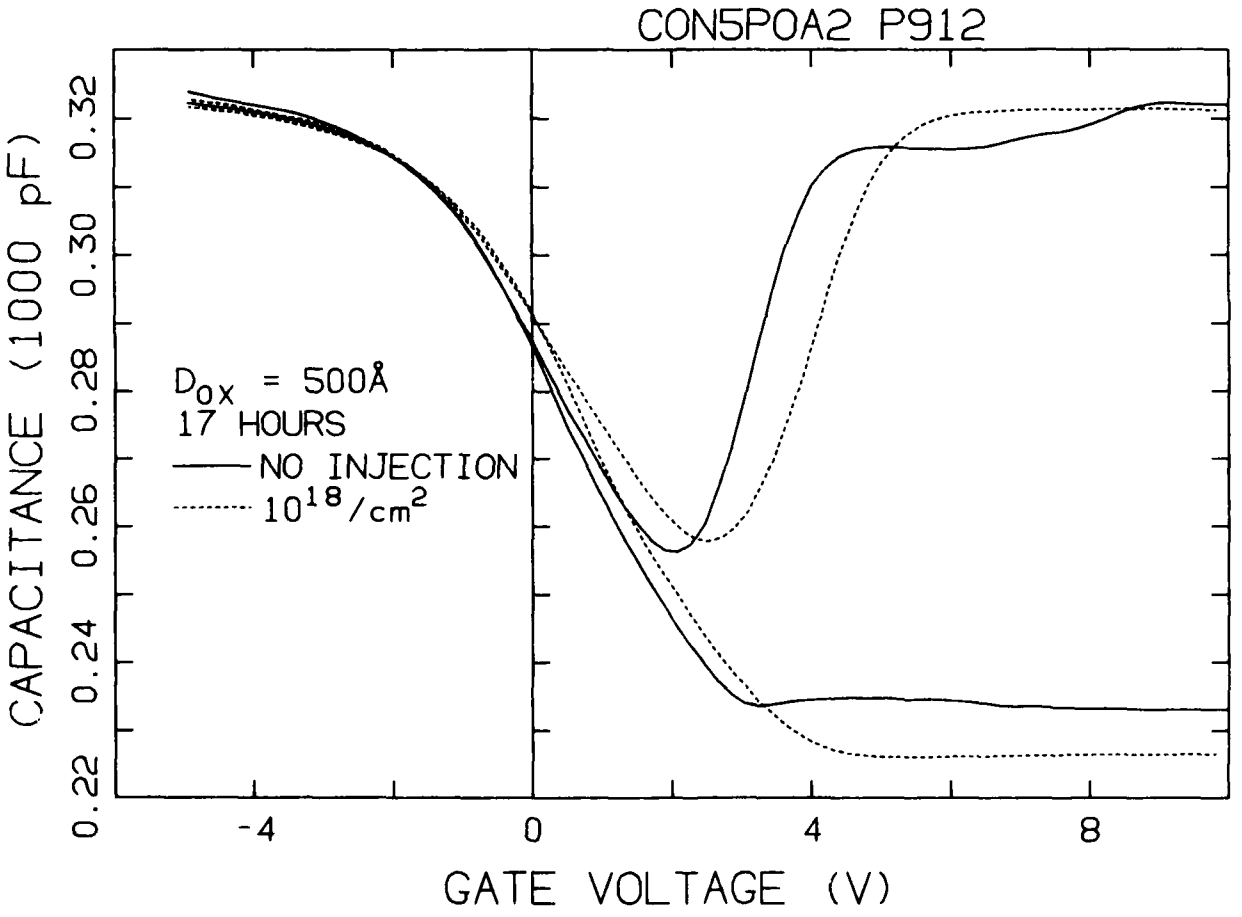

Fig. IV High frequency and quasistatic capacitance before and after injection of $10^{18}/cm^2$ electrons for an oxide that was annealed in nitrogen for 17 hours.

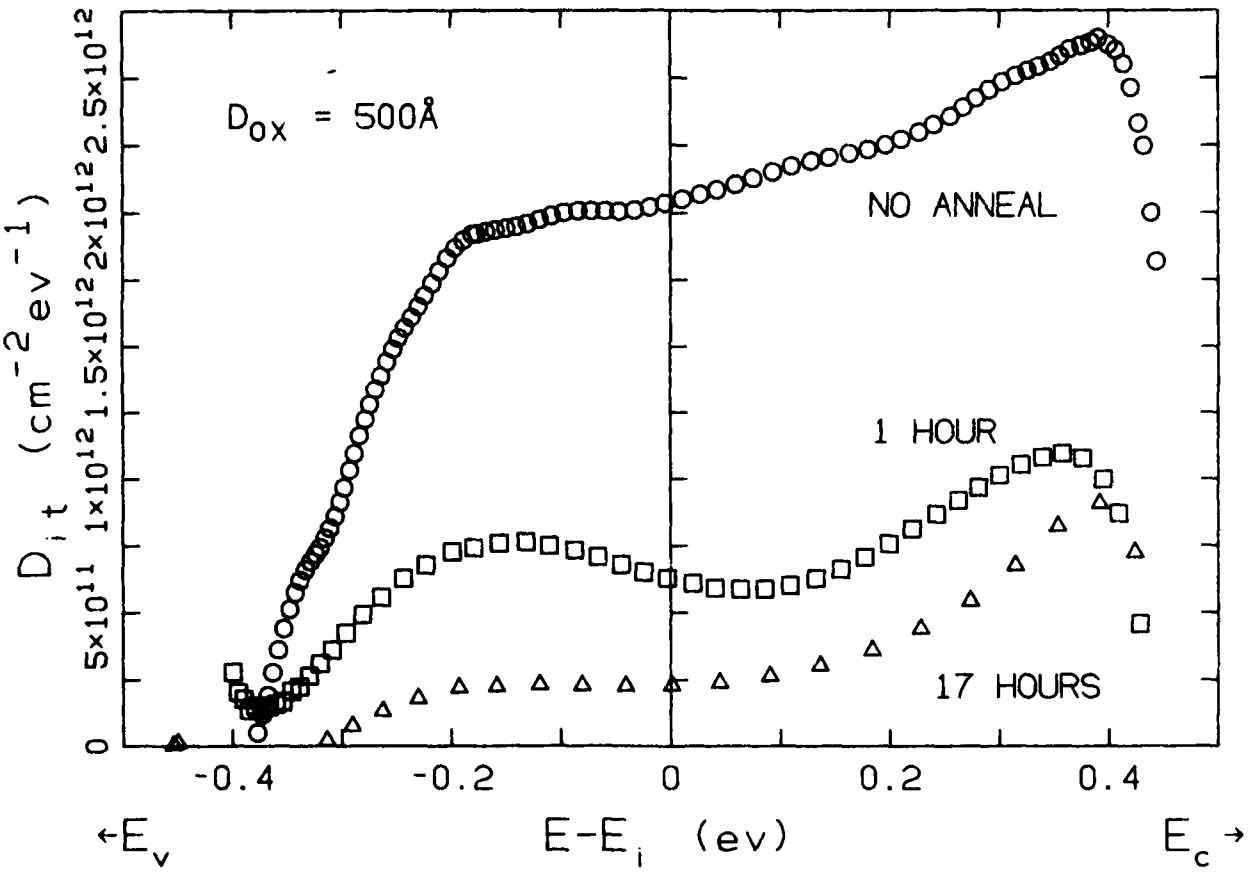

Fig. V Interface state densities after injection of $10^{18}/cm^2$ electrons for 500 Å oxides that are annealed in nitrogen for 0 hour, 1 hour and 17 hours, respectively. Any lateral nonuniformity effect has been ignored in the analysis and if the effect is large, these represent apparent interface state densities.

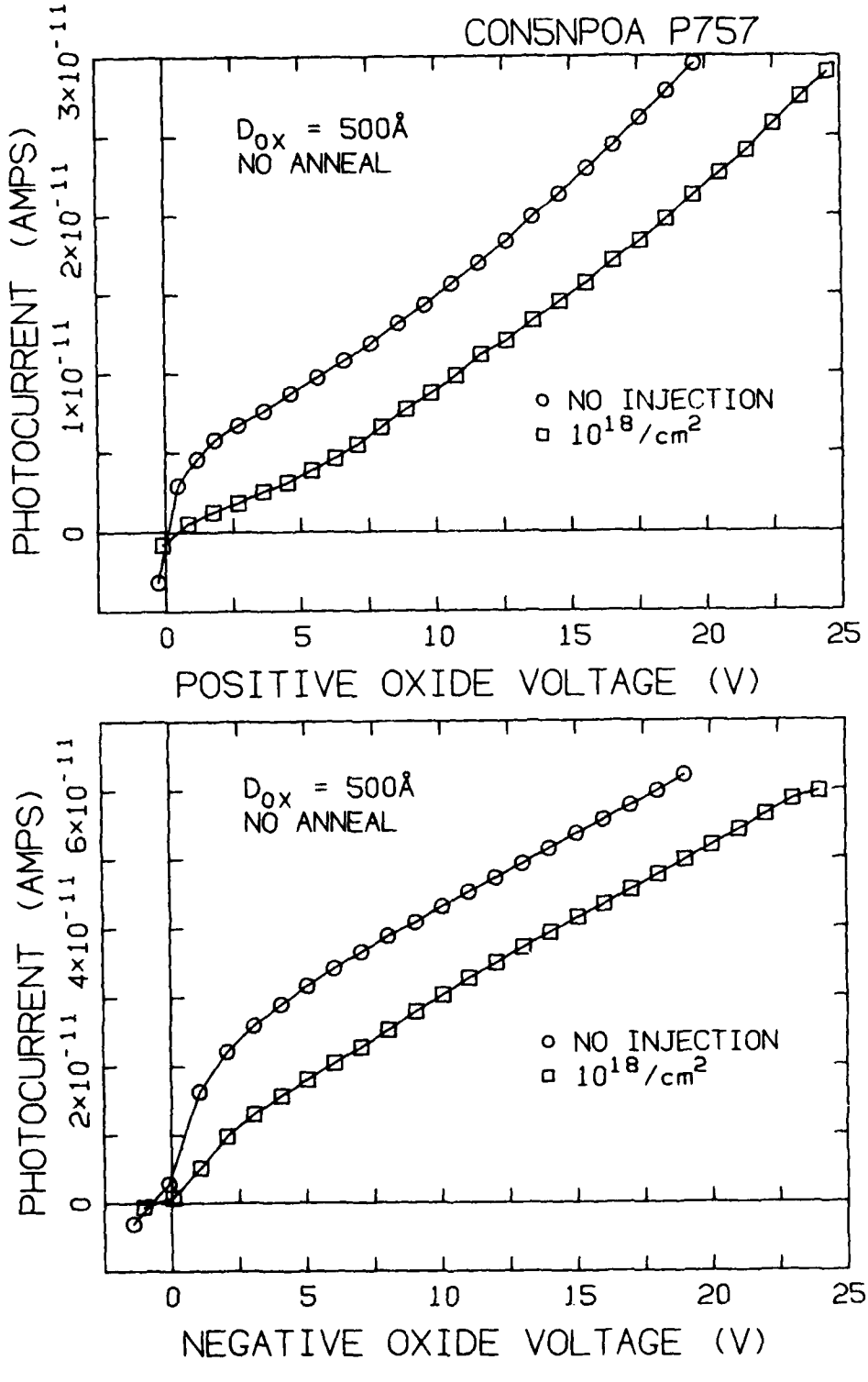

Fig. VI Photo I-V curves for before and after injection of 10^{18}/cm^2 electrons for an oxide that has not been annealed in nitrogen.

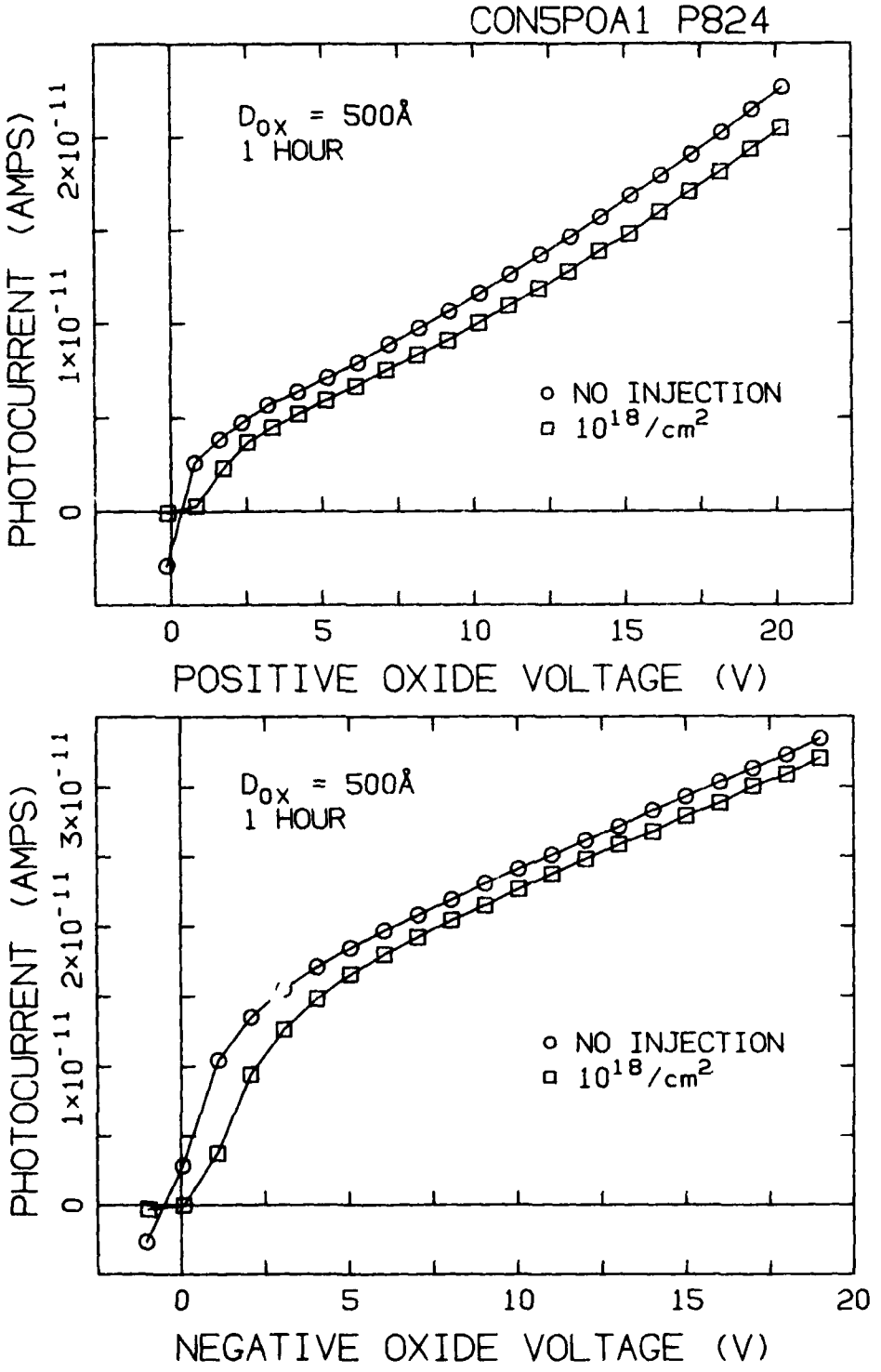

Fig. VII **Photo I-V curves for before and after injection of $10^{18}/cm^2$ electrons for an oxide that was annealed in nitrogen for 1 hour.**

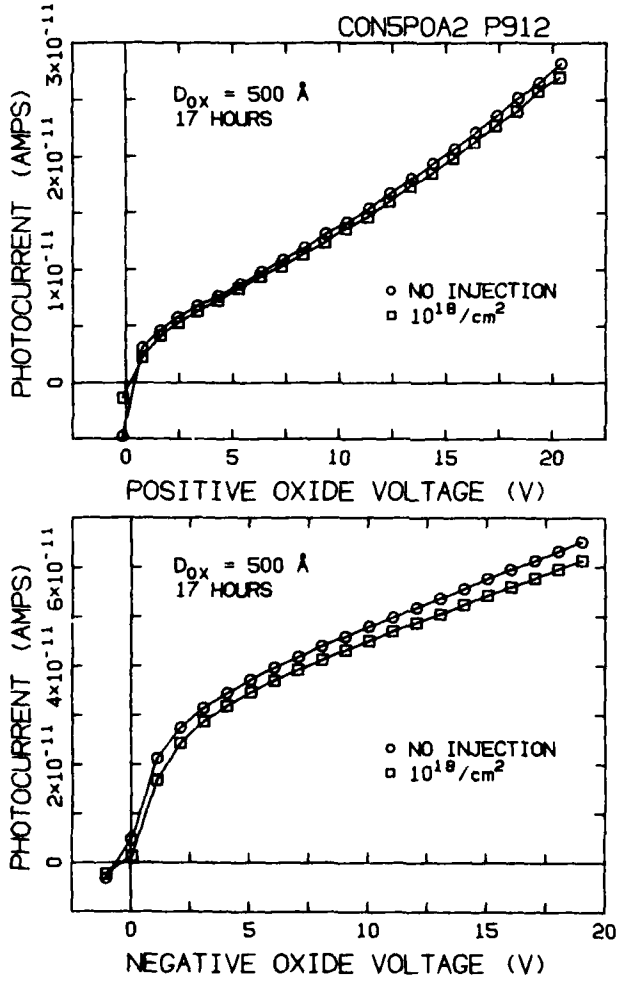

Fig. VIII Photo I-V curves for before and after injection of 10^{18}/cm^2 electrons for an oxide that was annealed in nitrogen for 17 hours.

HOLE TRAPPING IN E-BEAM IRRADIATED SiO_2 FILMS*

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Abstract

Low energy (25 kV) electron beam irradiation of MOS capacitors is shown to produce neutral hole traps in thin 'radiation hardened' SiO_2 films. These traps are found in an uncharged state after irradiation and are populated by passing a small hole current, generated by avalanche breakdown of the n-type silicon substrate, through the oxide. From the time dependence of the observed trapping, a capture cross-section between 1×10^{-13} and 1×10^{-14} cm^2 is deduced. The trap density is found to depend on the annealing conditions and incident electron beam dosage. The density of traps increases with incident electron beam exposure. Once introduced into the oxide by the radiation the traps can be removed by thermal anneals at temperatures above 500°C. Parallels between electron and hole trapping on these neutral centers are strong evidence for an amphoteric uncharged trap generated by ionizing radiation.

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Introduction

Electron and hole trapping in thin SiO_2 films has been the subject of a number of recent publications[1-9]. Trapping by holes and electrons at centers associated with ion implantation into SiO_2 films has been treated extensively[1-4]. Electron trapping at positive and neutral centers associated with ionizing radiation damage has also been discussed in connection with processes such as electron beam lithography[5,6], e-gun metal evaporation[7], or reactive ion etching[8]. Trapping of holes avalanche injected into as-grown SiO_2 films has also been treated[9]. This paper discusses hole trapping in SiO_2 at neutral centers created by ionizing radiation. It specifically addresses the effect of electron-beams in the 25 to 50 kV range on hole trapping in aluminum gate MOS capacitors. Empirical evidence that processing steps which expose gate oxides to ionizing radiation degrade the radiation hardness of those devices is well-known[10]. However the exact mechanisms of this phenomena have not been carefully studied. Previous studies use the radiation itself to generate holes to fill traps in the oxide and can generate additional traps in the process. This study uses radiation to create traps and subsequently fills them with holes electronically injected from the silicon substrate. This approach cleanly separates the trap generation and trap filling aspects of the problem. The existence of a neutral hole trapping center which is generated by ionizing radiation is verified. Its cross-section for hole capture, its dependence on electron beam dosage and its annealing temperature are reported. Experiments which locate the traps in the bulk of the film are also reported. The strong analogue which exists between neutral hole traps and neutral electron traps in irradiated oxides is discussed.

Experiment Description

Since this set of experiments was motivated by previous work in our laboratory involving neutral electron traps produced by ionizing radiation in thin SiO_2 films, the basic experimental procedures used in those experiments are repeated here[6]. The only significant difference

between the two sets of experiments is the use of n-type substrates to allow the injection of holes into the oxide instead of the p-type substrates used for electron injection.

The samples used in this experiment were MOS capacitors grown in dry O_2 at 1000°C on 0.1 Ω-cm n-type (100) silicon substrates. These oxide films were grown with a minimum number of hole traps by pulling the films directly from the oxide growth furnace without further annealing at this temperature. As shown in previous publications this procedure minimizes the trapping of avalanche injected holes in these oxides[10] and hardens them to the effects of ionizing radiation[9,11]. Two sets of samples with oxide thicknesses of 35 and 80 nm were grown. Aluminum contacts about 5×10^{-3} cm^2 in area were deposited in an r.f. evaporation system soon after oxide growth. This aluminum was 0.5 μm thick on most samples; on those used for photo-injection studies semitransparent metal about 10 nm thick was used. After aluminum deposition, the capacitors were annealed in forming gas for 20 minutes at 400°C to reduce surface states.

The MOS capacitors were exposed to various dosages of 25 or 50 kV electrons. These two energies were those available in the vector scan lithography system (25 kV) or the JEOL electron microscope (50kV). At these energies, the electrons penetrate the aluminum overlying the SiO_2 film and uniformly ionize the underlying oxide[12]. However, they are not energetic enough to cause lattice displacement damage. Electron beam dosages between 1 $\mu C/cm^2$ and 1000 $\mu C/cm^2$ were used. After being irradiated, the capacitors were annealed to remove the radiation-induced positive charge in the films[13]. However, some samples from the same wafer were irradiated but not annealed and conversely some annealed but not irradiated to provide controls. A small current of hot holes, generated by avalanche breakdown of the substrate, was passed through the oxide to fill the empty hole traps[9]. The change in flat-band voltage which occurs as a fraction of these holes are trapped in the oxide is automatically monitored as a function of injection time.

The avalanche injection system used in this experiment and its principles of operation have been described previously[9]. It is capable of generating a hot electron current in capacitors formed on p-type substrates and a hot hole current in those formed on n-type substrates. A special feedback circuit maintains the current at a chosen level by automatically adjusting the peak amplitude of a 50 kHz sawtooth voltage applied to the gate or substrate of the sample. This sawtooth waveform has been shown to be an important factor in the injection efficiency of the circuit[14].

Results

In the first experiment capacitors on the same wafer were exposed to various dosages of 25kV electrons and then annealed at 400°C for 20 minutes in forming gas. This anneal reduced the positive charge and surface state densities in all the capacitors to their pre-irradiation values. After annealing, their flat-band voltages were within 100 mV of each other and showed no dependence on dosage. Holes were then injected into the oxide at a constant current density of $8 \times 10^{-9} A/cm^2$. These traps are initially in a neutral state and are 'decorated' by injected holes which become trapped on them. The resultant change in flat-band voltage was recorded as a function of injection time and converted into an effective density of trapped charge by assuming that the charge is located only at the Si/SiO_2 interface. Since the current is maintained at a constant value by the feedback circuit, the elapsed injection time is directly proportional to the number of injected holes.

The results of this experiment are given in Fig. 1 where the change in flat-band voltage is plotted against elapsed injection time. The The effective density of holes trapped per unit area and the number of holes injected per unit area appear on the right hand and upper axes respectively. The electron beam dosage to which the capacitor was exposed is given adjacent to each of the curves. A control capacitor not exposed to the electron beam but subjected to the same anneal treatment is included in this figure for comparison. The additional 400°C

anneal received by the control sample in this experiment did not significantly change the hole trap density in the oxides from that present after the first anneal.

While no detailed analysis of trap cross-sections is presented here, the traps begin to reach saturation after 1×10^{14} holes/cm^2 have been injected into the oxide. The effective trapping cross-section is between 1×10^{-13} cm^{-2} and 1×10^{-14} cm^{-2}on this basis. As discussed by DiMaria, the assignment of this coulombic type capture cross-section to a neutral trap is in doubt[15]. These numbers more than likely overestimate of actual cross-section. Such overestimates arise either because holes which are trapped at the injecting interface are not included in the current measured in the external circuit or because the measured current is not simply related to the microscopic hole current[15].

As is also obvious from Fig. 1, a 400°C anneal does not remove the neutral hole traps from the oxide. The dependence of trap density on annealing temperature is shown in Table I. This table compares the trap density measured in irradiated capacitors as a function of various annealing conditions. The capacitors were exposed to a total flux of 1000μC/cm^2 25 kV electrons. The trap densities measured after 5×10^{14} holes/cm^2 had been injected into the oxide are shown along with the annealing temperature. The anneal was 20 minutes long and was performed in a forming gas ambient. Also included in the table are results for an irradiated capacitor which was not annealed and an unirradiated control which was. Note that the 500°C anneal does not reduce the trap density to its original level. Further attempts to anneal these capacitors at 550°C were unsuccessful because of oxide shorts. Radiation induced neutral electron traps also required temperatures above 550°C for complete removal[5,6].

Note that the increase in trapping is correlated with the total 25 kV electron exposure received by the sample. As in the case of neutral electron traps in irradiated SiO_2, the trap density increases with beam dosage. This point is illustrated in Fig. 2 where the flat-band voltage shift associated with a given electron beam dosage is plotted against that dosage. The

hole trap density was derived from Fig.1 by reading off the shift occurring after 1×10^{14} holes/cm^2 had been injected into the oxide. The hole trap density corresponding to this shift is also given on the right hand axis. At exposure levels below $5\mu C/cm^2$, the hole trap density is indistinguishable from that in the unirradiated samples as indicated by the dotted line. This behavior is similar to that reported for neutral electron traps. The shape of the curve describing the dosage dependence of neutral hole trap generation by electron beams is also similar to that for neutral electron traps generated under similar conditions[16].

The effective charge density shown in Fig. 1 is derived from a C-V measurement and is proportional to the first moment of the trapped hole distribution measured from the Si/SiO_2 interface. Photoemission measurements provide information on the first moment of the charge distribution from both interfaces. Separately or in conjunction with the C-V measurements they provide information on the location of charge trapped in SiO_2 films. Photoemission experiments have been used in the past to determine the centroid of trapped charge in oxides exposed to ion[3,4], photon[17], or electron beams[16]. Of particular interest to this work is the recent study of hole trapping in ion implanted oxide films in which holes were shown to be trapped in the bulk of the oxide film[4]. In the above paper hole traps were introduced into the oxide by ion implantation instead of with the electron beams used here. However the photoemission experiments used in the analysis are identical in procedure and interpretation regardless of the source of the hole traps. A detailed treatment of centroid determination in the presence of holes trapped in the bulk is available in this reference.

Figure 3 displays the photoemission curves generated using the aluminum as the source of photoelectrons generated by 4 eV light. As discussed in reference 4, this choice of injecting electrode and photon energy minimizes the complications of interpretation associated with double injection phenomena. Such phenomena are caused by the large fields at the interfaces associated with the presence of charge in the oxide. This particular sample was irradiated with 50 kV electrons and after irradiation was annealed at 400°C in forming gas to reduce the

radiation induced positive charge. In addition this anneal removes some of the neutral hole trapping centers in the film. Photoemission current measurements were taken prior to hole injection, after hole injection and after electrons were injected into the oxide to partially annihilate the trapped hole distribution. Note the distortion of the characteristic in the low field region after hole injection. This distortion is due principally to the recombination of injected photoelectrons with the trapped holes in the oxide during the measurement. The recombination results in a displacement current which subtracts from the photocurrent. It is important to note that the displacement current is due to the annihilation of holes which are to a large extent ***removed from the Si/SiO_2 interface***. Annihilation of holes at this interface would not result in any displacement current[4].

The other important feature in this curve is the voltage necessary to suppress injection from the of photoelectrons from the Al contact. This is called the cross-over voltage and is related to the voltage necessary to establish the flat-band condition at the Al/SiO_2 interface. When the applied voltage is sufficient to compensate the internal field at the aluminum interface, injection from this interface stops and the current goes to zero. As discussed in reference 4, the cross-over voltage observed in this figure is indicative of a large positive charge distribution in the bulk of the film.

On continued injection of photoelectrons the photo-emission characteristic relaxes back to its initial state as the holes trapped in the oxide are annihilated by the injected photoelectrons. By biasing the capacitor at the silicon flat-band condition this recombination takes place selectively at the silicon interface[4]. This effect was exploited to selectively remove charge at the silicon interface leaving principally bulk trapped positive charge. In this case the shift in the aluminum photoemission characteristic was identical to that measured from the C-V curves. This combination of shifts is also consistent with charge trapped in the middle of the film[4].

To show that neutral electron traps also co-exist in these films, electrons were photoinjected into them prior to any hole injection. In this case also the photoemission data indicated neutral electron traps whose centroid is in the middle of the film.

Conclusions

The neutral hole traps introduced into the SiO_2 layers have many of the same signatures as neutral electron traps generated by electron beam irradiation. They have the same type of dosage dependence, anneal at the same temperatures and have a centroid in the middle of the oxide. As mentioned above both neutral electron and hole traps exist simultaneously in the same oxide after irradiation. When integrated over a large range of capture cross-sections, the total number of hole and electron traps are also comparable. While it is difficult to prove directly, these facts suggest that the same trapping centers are responsible for the capture of holes and electrons in these samples. The dipolar trapping center discussed earlier in connection with radiation - induced neutral traps is also applicable to hole traps as well[6]. Such dipoles may consist of positively and negatively charge regions which arise from bonds broken during the bombardment with energetic electrons. These centers would not effect the field at the SiO_2/Si interface since the field associated with it goes to zero in a short distance away from the center. However carriers which come close enough to the center may be permanently captured. The positively charged regions act as efficient electron traps while the negatively charged regions act to trap holes. The capture cross-sections for these traps would depend on the exact spatial distribution of the electrons associated with the broken bond.

From a practical point of view these results show that ionizing radiation increases the density of hole traps in radiation-hardened SiO_2 However a large fraction of these traps are located in the bulk of the oxide and not at the interfaces. The results suggest that the mechanism by which hardness is degraded is the creation of additional hole traps in the oxide. It is not clear at this point whether it is the interfacial or bulk traps that are responsible for the degradation. The bulk centers apparently do not charge during exposure to ionizing

radiation. Irradiation produces equal numbers of electrons and holes in the oxide while avalanche injection is a single carrier process. Once a center is formed by interaction with radiation it can trap either a hole or an electron. This charged center is prone to be neutralized by the carrier of opposite sign. In experiments where a single carrier is injected, the possibility of recombination is automatically greatly reduced and allows charge to accumulate in the bulk.

Acknowledgements

The authors wish to thank D.R. Young for his continued interest, suggestions, and support during the course of this work. Sample fabrication was done by the Silicon Process Studies Group; irradiations were done by the Electron Beam Lithography Applications Group and C.M. Serrano. The help of these groups and individuals is gratefully acknowledged.

TABLE I

EFFECT OF ANNEAL TEMPERATURE ON TRAP DENSITIES IN IRRADIATED[a] CAPACITORS

ANNEAL[b] TEMPERATURE (°C)	EFFECTIVE DENSITY OF FILLED TRAPS[c] (cm^{-2})
NO ANNEAL	3.2×10^{12}
400	2.6×10^{12}
450	2.2×10^{12}
500	1.6×10^{12}
No E-beam 400	0.3×10^{12}

a) $1000\mu C/cm^2$; 25 keV electrons

b) 20 min in forming gas

c) After injection of 5×10^{14} holes/cmu2

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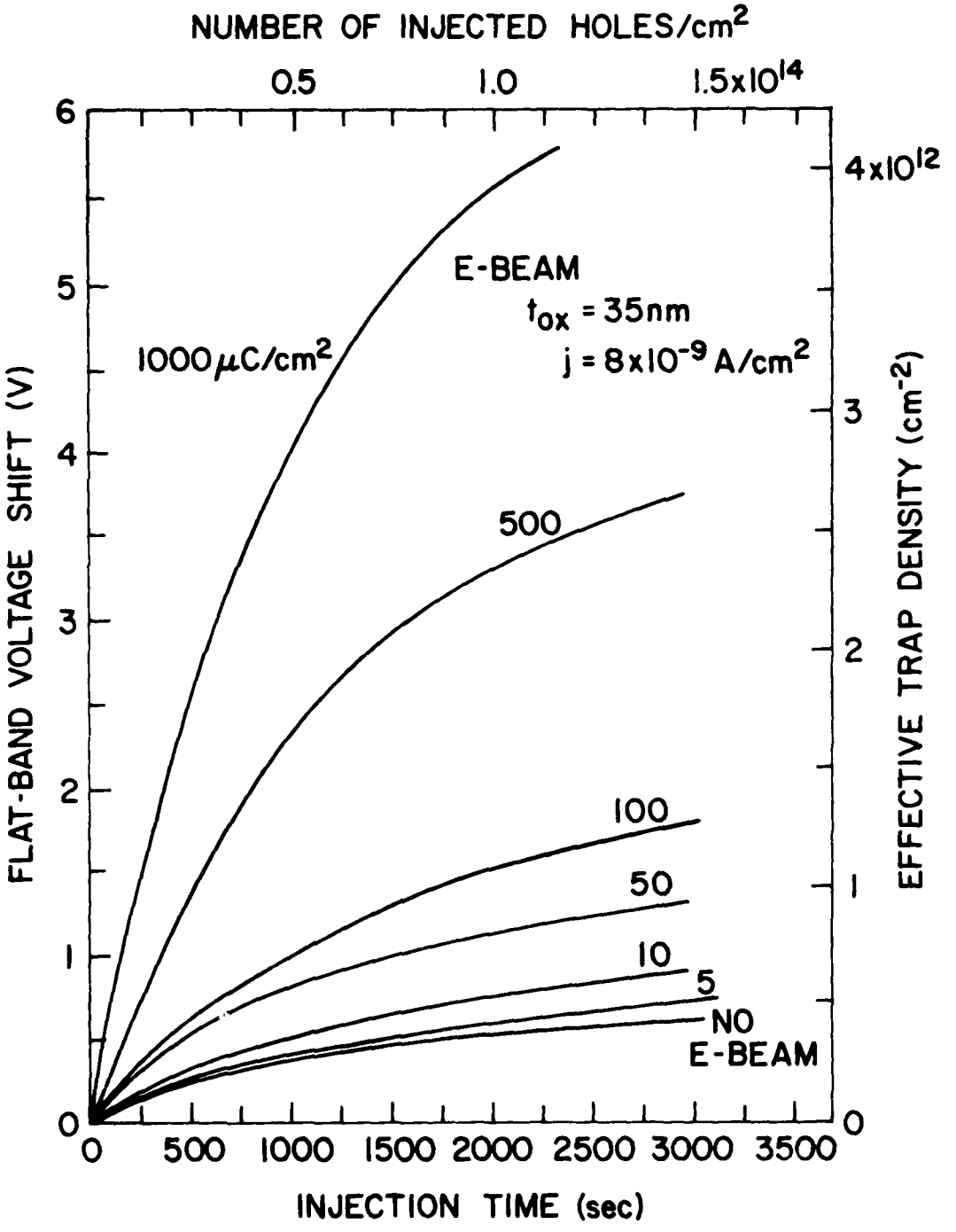

Fig. 1. Flat-band voltage shift (effective trap density) observed as a function of injection time (number of injected holes/cm^2) for MOS capacitors subjected to various dosages of ionizing radiation. These samples were annealed at 400°C after irradiation.

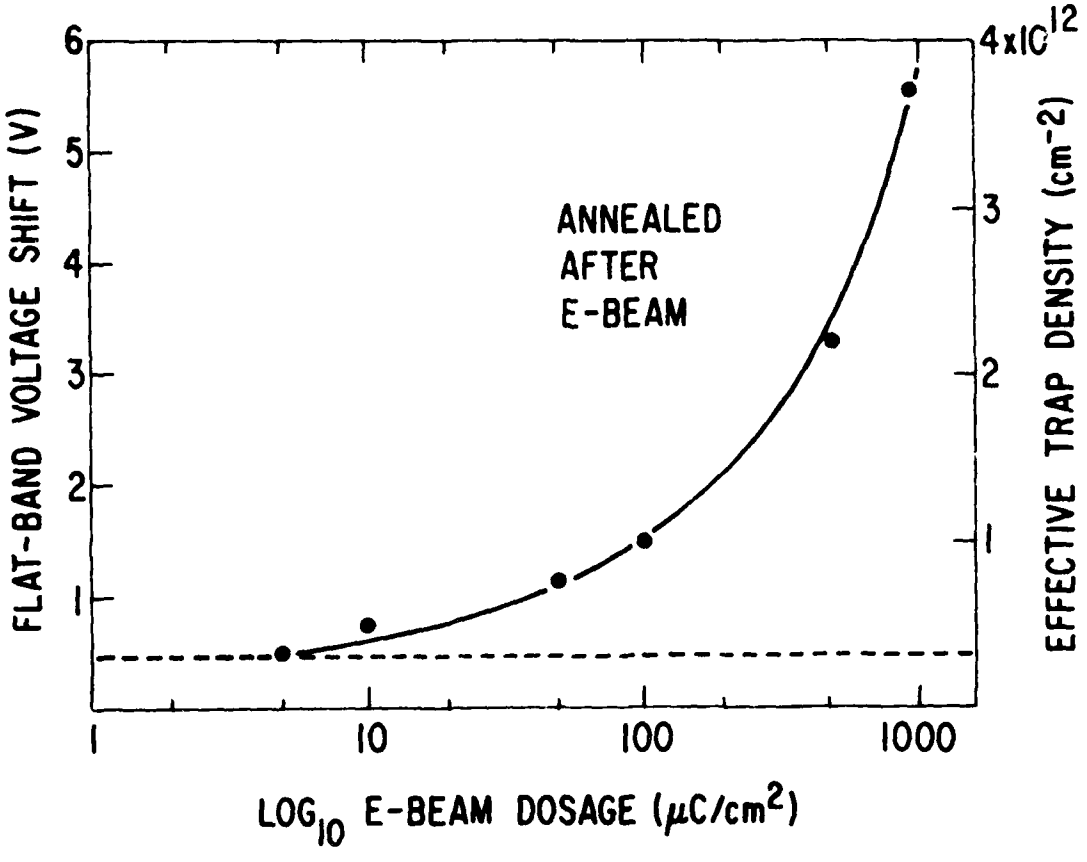

Fig. 2. The flat-band voltage shift (effective trap density) observed after 1×10^{14} holes/cm^2 have been injected through the capacitors. The flat dotted line indicates the level of traps observed in the as-grown oxide.

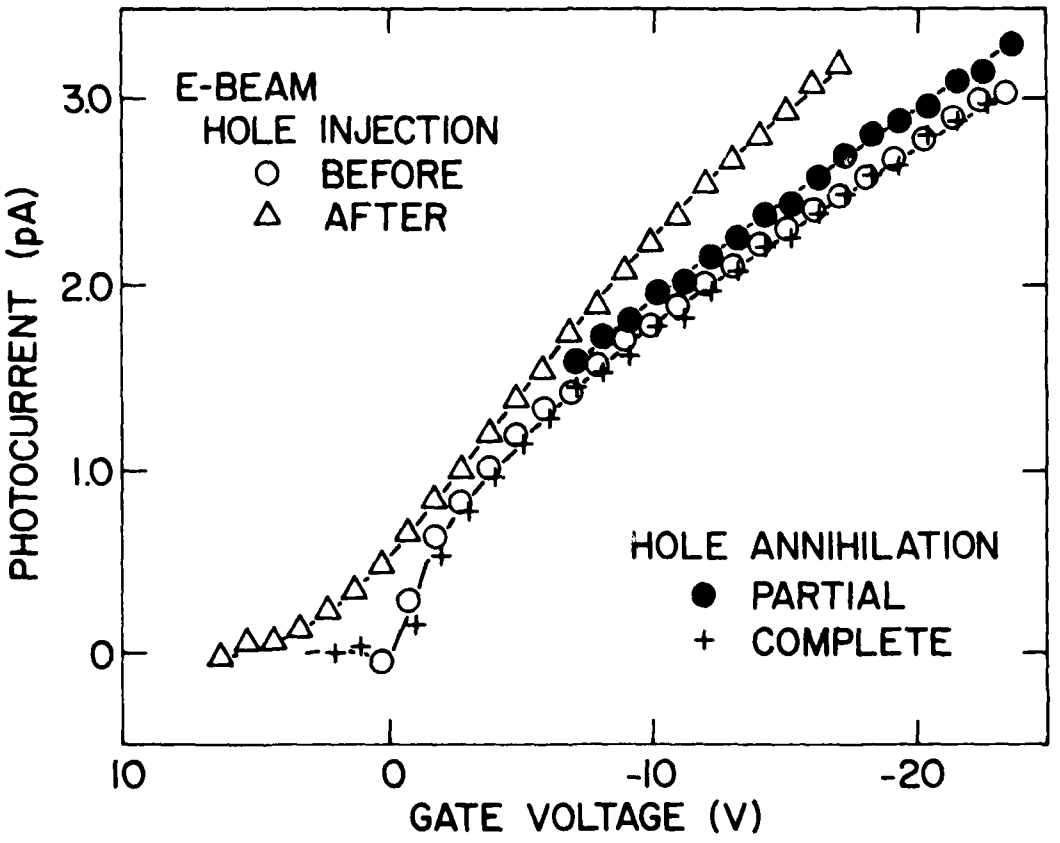

Fig. 3. Photoemission current versus gate voltage for sample measured before and after holes were injected into the oxide and after these holes have been annihilated by photo-injected electrons. The oxide was 80.0 μm thick. Samples was annealed after exposure to 50 KV electrons.

THE EFFECTS OF WATER ON OXIDE AND INTERFACE TRAPPED CHARGE GENERATION IN THERMAL SiO_2 FILMS

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ABSTRACT

Water was diffused into very dry thermal SiO_2 films under conditions such that the penetration of water related electron trapping centers was of the order of the oxide thickness. In both dry oxides and water diffused oxides, production of negative bulk oxide charge Q_{ot} and positive interface charge Q_{it} by an avalanche-injected electron flux was observed. The efficiencies of both processes were enhanced by water indiffusion. Analysis of the kinetics of charge generation indicated that production of trapped electron centers (Q_{ot}) was required for subsequent production of interface states and charge (Q_{it}). Models for both processes are discussed. We suggest that inelastic collisions of conduction electrons with the trapped electron centers releases mobile hydrogen atoms or excitons. The mobile species migrate to the Si-SiO_2 interface and form states and fixed charge.

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I. INTRODUCTION

Recent major developments within the silicon planar technology have renewed interest in an old problem -- charge carrier capture and localization at impurity, dopant, or defect centers in thin oxide films. This phenomenon was first reported by Williams in 1965 (1). The charge buildup associated with such electron and hole trapping improves dielectric breakdown characteristics of insulating films, adversely affects the long term stability of short channel devices in VLSI technology and of floating gate switching in electrically alterable memory devices, and generally complicates electron, x-ray, and particle beam technology. Recent reviews on electron and hole trapping in oxide layers have been published by DiMaria (2), Young (3), and Aitken (4).

Negative oxide charge buildup produced by trapping of electrons injected into oxide films was studied under carefully controlled conditions by Nicollian and coworkers (5). These investigators prepared dry thermal SiO_2 films which contained a low density of coulomb-attractive or electrically neutral trapping centers. Diffusion of water into these films at low temperatures greatly enhanced electron trapping. The dominant trapping center had a capture cross section of approximately 1.5×10^{-17} cm^2. The total density of these trapping centers was asserted to be proportional to the water content of the films. This association was indirect, and applied only in the limit in which the oxide film thickness greatly exceeded the water diffusion depth.

Nicollian and coworkers (5-7) also studied the formation of interface states by passage of an injected electron current. This process is also enhanced by the presence of water in the oxide film. Specifically, Nicollian and coworkers indicated that the interface states are not produced in dry grown oxides subjected to post oxidation water diffusion unless the diffusing species reaches the $Si-SiO_2$ interface.

The early Bell Laboratory studies just described were complemented by numerous subsequent investigations of electron trapping in very dry oxide films, nominally dry oxide films prepared by current industrial techniques (and possibly subject to unintentional water contamination at high and/or low temperatures), and wet thermal oxide films (produced by oxidation of silicon in water containing ambients). This work has been reviewed in detail (2-4). Dry oxide films have been shown to exhibit significant electron trapping. However, trapping in dry oxide films is much less efficient than trapping in oxide films containing water. All water-containing films have a dominant trap (or traps) with cross section(s) in the range 10^{-17}-10^{-16}cm^2. Dry oxide films have dominant traps with effective cross sections of order 10^{-18}cm^2 or less.

Gdula (8) reported a buildup of positive charge in water-containing oxide films subjected to electron avalanche injection for extended times. In his studies, and in subsequent work by other investigators (9,10), this anomalous positive charge buildup appeared to occur beyond a transported electron fluence threshold of approximately 0.01 C-cm^{-2}. Young and coworkers demonstrated that this positive charge was located at the Si-SiO_2 interface, and that, once generated, it could be significantly altered by variations of electric field and/or temperature without current injection (10). These results indicated that the anomalous positive charge was in fact produced by ionization of donor-like interface states in electrical and thermal communication with the silicon surface, and was not "fixed" in the oxide layer. This model was subsequently verified in detail by Miura and coworkers (11). It thus appears likely that the anomalous positive charge effect is at least partly related to the interface state generation reported by Nicollian and coworkers (5-7).

The purpose of the present study was to examine in more detail the low temperature diffusion of water into dry thermal oxide films. We have

concentrated on the regime in which the anomalous positive charge effect occurs. We have prepared dry oxide films at 1000°C, using the oxidation procedures developed by E. A. Irene (12), and have diffused water into these films at low temperatures (100-300°C), using procedures described by Nicollian and coworkers (5). Both dry control oxides and water diffused oxides were incorporated into p-substrate metal-oxide-semiconductor (MOS) capacitor structures. These devices were subjected to avalanche electron current injection, and the net oxide and interface charge induced during passage of the electron currents across the oxide was measured under a variety of experimental conditions. Recent instrumentation and data analysis developments were used to separate the negative charge buildup caused by electron trapping in the bulk of the oxide films from the positive charge buildup in the $Si-SiO_2$ interface region.

Both negative oxide charge buildup and positive interface charge buildup were observed in dry oxide films and in water-diffused oxide films. The efficiencies of both processes, relative to the injected electron current flux, were one order of magnitude lower in the dry oxide films than they were in the water-diffused oxides. In both types of films, detailed kinetic studies indicate that formation of trapped-electron centers (and buildup of negative oxide charge) must occur before formation of positive charge at the $Si-SiO_2$ interface can occur. In addition, the formation of donor-like interface states and fixed oxide charge responsible for measured positive interface charge requires a second kinetic step initiated by the injected electron flux, other than the original electron capture.

II. EXPERIMENTAL PROCEDURES

A. Sample Preparation

The general details of sample preparation have been described by Young et al. (9). Polished, (100), p-type silicon wafers with a nominal resistivity of 0.2 Ω-cm were oxidized in a three-zone resistance furnace (12). Oxidations were carried out at 1000°C, using oxygen supplied from a liquid source. Hydrocarbons were removed from the oxygen gas, and the H_2O content of the dried O_2 gas leaving the oxidation furnace was <1 ppm (12).
Oxidized samples were left in the furnace and maintained at 1000°C for at least twenty minutes after the O_2 was turned off. Dried N_2 gas was flowing during this post-oxidation annealing step.

In the later stages of this study, sample oxidations were preceded by a flush of the oxidation furnace for several hours in dried N_2 gas. In addition, some samples were cooled to handling temperature under a continuous dry N_2 flush after the post oxidation annealing treatment described above. These steps were taken to reduce the trapping rate attributable to H_2O impurities in the oxide film.

The SiO_2 film thicknesses used for this study were in the range 384-2440 Å. Thicknesses were measured by ellipsometry.

After the oxidation step, most of the oxidized wafers were divided. Individual research samples (half or quarter wafers) were placed inside a diffusion furnace in a clean, dry, flowing nitrogen ambient. Once the temperature of the furnace stabilized at the desired diffusion temperature, the clean N_2 gas was switched to an alternate line that included a controlled-temperature deionized water bubbler in series with the diffusion furnace tube. The N_2 flow rate was reduced to maximize the H_2O content of the bubbler effluent; only a slight overpressure was maintained within the gas line and

furnace tube to exclude ambient air. All connecting lines between the bubbler and the heated zone of the furnace tube were maintained above 100°C to prevent water condensation. The water diffusion system was intended to be identical to that described by Nicollian and coworkers (5). Further details are available in reference 5.

The low temperature water diffusion step was usually 10 minutes in duration. Diffusion was initiated by switching the gas flow from dry to wet N_2, and was terminated by the reverse procedure. Water diffusion was done at diffusion (sample) temperatures in the range 135-300°C, and at bubbler temperatures in the range 30-60°C. For the bubbler temperatures quoted, nominal (saturated) water vapor pressures are approximately 50-150 mm Hg. After a diffusion step, samples were removed from the furnace hot zone and cooled to handling temperature in a flowing dry N_2 ambient.

Immediately after diffusion, 100-200 Å thick Al electrodes, typically 0.032 in. diameter, were evaporated onto the SiO_2-Si structure from a borosilicate crucible which was heated by rf induction. The oxide on the back side of the silicon was etched off and a gallium indium paste was used for back side electrical contact.

Except as specifically noted, no postmetallization annealing was performed on samples used in this study. The effect of water indiffusion on charge trapping and donor state generation was the object of this study. Young and coworkers (9) have shown that postmetallization annealing reduces the trapping phenomenon, and in fact eliminates certain traps suspected of being water-related.

The overall cleanliness of the entire sample preparation process was assessed by performing C-V measurements and bias-temperature-stress measurements on control MOS devices, as previously described (9). For each diffusion

sequence, a control sample was metallized immediately after the oxidation step. In addition, for selected diffusion sequences, at least one partial wafer was maintained as a control. The control sample for each selected diffusion step was stored in a dry, clean, flowing N_2 ambient until the diffusion step was completed. The control and the H_2O diffused sample were then simultantously metallized, as described above.

B. Measurement Procedure

Electron trapping and electron transport induced positive charge build-up in both control oxide and diffused oxide MOS capacitors were examined using the constant current rf avalanche method developed by Young (9). This technique is a refinement of the avalanche injection technique developed by Nicollian, Goetzberger, and Berglund (13,5). Pulsed electron flow is induced through the SiO_2 film by rf avalanche in the p-silicon surface depletion layer, and the rf voltage level V_A is continuously adjusted to maintain a constant average dc current I_A throughout a given run. The high frequency C-V flat band voltage V_{FB} is automatically monitored and recorded at preset intervals throughout the run. Details of the instrumentation are described by Young and coworkers (9).

The basic experimental data in this program is ΔV_{FB} as a function of cumulative avalanche injection time t_A. The flat band voltage shift ΔV_{FB} is given by $\Delta V_{FB}(t_A) = V_{FB}(t_A) - V_{FB}(t_A=0)$, where $V_{FB}(0)$ is the flat band voltage of the sample as prepared, before any avalanche injection. These data are most often presented as plots of ΔV_{FB} vs F_A, where $F_A \equiv I_A t_A/A$ is the integrated current density, with units $C\text{-}cm^{-2}$, over a given run. Such data are shown in Figure 1 for a dry (control) oxide device and for an H_2O diffused oxide device.

In many cases, such runs were made both with the device maintained at room temperature, as in Figure 1, and with the device maintained at approximately 100°C. These runs were made on separate electrodes on a given sample. Examples are presented in Figures 2 and 3, for a dry control and a diffused oxide sample, respectively.

On selected samples, we have augmented the flat band voltage shift measurements with measurements of other MOS capacitor device characteristic shifts. The rf avalanche voltage V_A has been recorded throughout an avalanche injection run, and the shift of this voltage, ΔV_A, has been determined as a function of t_A or, equivalently, F_A. In these experiments, the avalanche injection run has been interrupted at selected points and the photo I-V characteristic of the MOS device has been measured. The internal photoemission I-V apparatus and procedures of DiMaria have been used for these experiments. Details have been presented by DiMaria (2,14).

All measurements of ΔV_A and photo IV characteristics were executed with the sample maintained at room temperature. Typical data obtained in these experiments -- ΔV_{FB}, ΔV_A, and ΔV_p^+ as a function of t_A or F_A -- are illustrated in Figure 4 for a dry control oxide sample and two different H_2O diffused oxide samples. V_p^+ is the shift of the measured photoemission I-V characteristic shift under positive gate bias (2,14). ΔV_p^-, the photo I-V characteristic shift under negative gate bias, has also been measured for each sample. All results of these measurements reported below satisfied the criterion that the avalanche voltage shift ΔV_A and the photo I-V voltage shift ΔV_p^+ were identical within the overall precision of the separate measurements. The importance of this will be discussed below.

C. Data Analysis Procedures

Trapping data obtained in the experiments described above were analyzed in terms of a multiple trap model, with first order trapping kinetics. A single trapping center was characterized by an effective capture cross section for electrons, $\sigma_{ci}(cm^2)$, and an areal trap density $N_i(cm^{-2})$. For one trapping center, the negative charge buildup associated with electron capture is

$$Q_i(t_A) = -eN_i[1-\exp(-\frac{1}{e}F_A\sigma_{ci})]. \quad (1)$$

F_A is the integrated charge fluence during avalanche induced electron transport across the SiO_2 film, and is proportional to t_A. e is the magnitude of the electronic charge, 1.6×10^{-19} C. The total negative trapped charge in a sample at time t_A is a sum over all trapping centers

$$Q(t_A) = \sum_i Q_i(t_A) \ . \quad (2)$$

An experimental determination of $Q(t_A)$ vs. F_A, or of related quantities as defined below, can therefore be analyzed by mathematical deconvolution or simulation of the experimental curve in terms of a sum of exponential terms with different amplitudes (eN_i) and different characteristic rates (σ_{ci}/e). The resulting best-fit parameters have a simple physical interpretation as the density and capture cross section of trapping centers, located either in the bulk of the SiO_2 film or at one of the solid-solid interfaces of the MOS structure. Young and coworkers have discussed the fitting procedure, and their paper should be consulted for details (9).

The overall data measurement and analysis procedures employed in this study can reliably discriminate between trapping centers which differ by less than a factor of 100 in trap density N_i and more than a factor of 4 in cross section σ_{ci}, if the appropriate range of charge fluence F_A is examined. The

correlation between trapping cross section and the charge fluence is obvious from Equation 1, and is summarized in Table 1. This table is useful for qualitative analysis of experimental data whenever manifest breaks occur in the Q vs. F_A or ΔV vs. F_A curves.

The data of Figure 5, for example, indicate that the diffused oxide and both of the dry oxides all contain similar amounts of very small cross section traps (10^{-20}-10^{-19} cm^2). Both of the dry oxides, however, have a 2-3 volt flat band shift associated with traps having cross sections in the range 10^{-18} cm^2. The main differences among the several experimental curves occur at short times (small fluences). The PMA dry oxide exhibits very little trapping with $\sigma_c \sim 10^{-17}$ cm^2. The dry oxide sample without PMA does contain 10^{-17} cm^2 cross section traps, which produce a voltage shift of approximately 1 volt. The H_2O diffused oxide, however, exhibits a flat band shift of 3-4 volts for $F_A \sim 0.03$ C-cm^{-2}. Obviously, H_2O diffusion strongly enhances the amount of negative charge buildup due to traps with $\sigma_c \sim 10^{-17}$ cm^2, and post metallization annealing reduces such trapping. These qualitative conclusions agree with the results of Young and coworkers (see Figure 2 of reference 9).

Refinement of these conclusions requires detailed quantitative analysis of the experimental data, as discussed above, using Equations (1) and (2). Such analysis, for example, reveals a small amount of traps with $\sigma_c \sim 10^{-18}$ cm^2 in the H_2O diffused oxide.

A major complication of this simple picture is the anomalous positive charge effect, illustrated in Figures 2 and 3 for both a dry control oxide and a water diffused oxide. The ΔV_{FB} data obtained at 22°C shows clearly the flat band shift reversal associated with positive charge production

at the $Si-SiO_2$ interface. The ΔV_{FB} data obtained at 100°C does not show this effect, as previously reported by Young and coworkers for non-diffused oxides (9).

Unless the detailed kinetics of the anomalous positive charge phenomenon can be established, this effect will interfere with the quantitative analysis of trapping. Comparison of ΔV_{FB} data at 22°C and 100°C in Figures 2 and 3 clearly indicates that N_i and σ_{ci} obtained from 22°C flat band shift data in the regions $F_A < 0.03 C\text{-}cm^{-2}$ and $F_A = (0.2\text{-}1.0) C\text{-}cm^{-2}$ would be highly suspect, unless corrections were made for the anomalous positive charge buildup.

In nominally dry oxides, it is clear that the anomalous positive charge is located in the immediate vicinity of the $Si-SiO_2$ interface (9). This fact provides a basis for separation of the negative charge buildup due to electron trapping from the positive charge anomaly associated with the build-up of interface charge and states. First, as illustrated in Figures 2 and 3 and as discussed by Young, et al. (9), C-V flat band shift measurements under positive bias at elevated temperatures (~100°C) can be interpreted in terms of bulk trapping only. Second, photo I-V shifts ΔV_p are not sensitive to interface charges, and provide an independent measure of the bulk charge due to electron trapping. This has been discussed by Powell and Berglund (15), and by DiMaria (2,14). Third, and finally, variations of the rf avalanche voltage shift ΔV_A were demonstrated to follow variations of the photo I-V characteristic shift under positive bias, ΔV_p^+. This was illustrated in Figure 4, and is further demonstrated by the results in Table 2. ΔV_A is thus also useful as a measure of bulk charge trapping. V_A was used by Nicollian and coworkers (5,7) for this purpose. The procedure does have an

explicit theoretical basis in the analysis of Nicollian and Berglund (7). However, the procedure has been questioned by other investigators (9). In the present case, use of ΔV_A is justified by the comparison with ΔV_p^+, and these two measurements are complementary rather than independent.

The following equations summarize the interpretation of experimental measurements described above.

$$\Delta V_{FB}(RT) = -\frac{1}{C_{ox}}(Q_{ot} + Q_{it}) \tag{3}$$

$$\Delta V_{FB}(HT) = \Delta V_p^+ \approx \Delta V_A = -\frac{1}{C_{ox}} Q_{ot} \tag{4}$$

RT means measurement with the sample maintained at room temperature (22°C); HT means measurement at high temperature (∿100°C). C_{ox} is the MOS device oxide capacitance $K_{SiO_2}\varepsilon_o \cdot A \cdot d_{ox}^{-1}$, where $K_{SiO_2}\varepsilon_o$ is the dielectric permittivity of amorphous SiO_2. Q_{ot} is the centroid weighted oxide trapped charge, given by

$$Q_{ot} = d_{ox}^{-1} \int_{0'}^{d'_{ox}} x\rho(x)dx, \tag{5}$$

where $\rho(x)$ is a volume density of trapped charge (C-cm^{-3}) and the primes on the integral limits explicitly indicate exclusion of the solid-solid interface regions, in line with the convention proposed by Deal (16). Q_{it} is the net interface region charge, consisting of the component of oxide trapped charge produced by the avalanche process in the immediate vicinity of the Si-SiO_2 interface plus an integral over interface state charge D_{it} (ionized donor states) appropriate to measurement at flat band voltage. We have not attempted to separate these contributions. This point will be discussed further below.

Equations (3) and (4) yield the following relations used to analyze experimental data.

$$N_{ot} = Q_{ot}/e = \frac{1}{e} C_{ox} \Delta V_{FB}(Ht) \tag{6A}$$

$$= \frac{1}{e} C_{ox} \Delta V_p^+ \tag{6B}$$

$$= \frac{1}{e} C_{ox} \Delta V_A \tag{6C}$$

$$N_{it} = Q_{it}/e = \frac{1}{e} C_{ox} [\Delta V_{FB}(HT) - \Delta V_{FB}(RT)] \tag{7A}$$

$$= \frac{1}{e} C_{ox} [\Delta V_p^+ - \Delta V_{FB}(RT)] \tag{7B}$$

$$= \frac{1}{e} C_{ox} [\Delta V_A - \Delta V_{FB}(RT)] \tag{7C}$$

The comparison of room temperature flat band shifts $\Delta V_{FB}(RT)$ with other measured quantities required by Equations (7A)-(7B) is partly justified by the observation that the several measurements all have identical initial slopes. This is illustrated in Figures 2-5 and in Figure 6. Equations (1) and (2) indicate that the initial slope of the trapping curve (Q vs. F_A) is the sum of the initial electron capture efficiencies $\eta_i(0) = N_i \sigma_{ci}$ of the individual trapping centers. Thus

$$\left|\frac{dQ}{dF_A}\right|_{F_A=0} = \sum_i \eta_i(0) = \sum_i N_i \sigma_{ci} \ . \tag{8}$$

The similarity of initial trapping rates in ΔV_A and $\Delta V_{FB}(RT)$ data indicate that the anomalous positive charge buildup rate is small compared to the net trapping rate initially. The similarity of initial trapping rates in $\Delta V_{FB}(RT)$ and $\Delta V_{FB}(HT)$ data indicates that temperature variations do not have a large effect on the trapping parameters.

In addition, high temperature treatment did not significantly alter the charge trapping behavior of the samples studied. Figure 7 shows

ΔV_{FB} vs t_A data obtained on a dry control sample. Extensive voltage cycling was performed on this sample between the HT measurement and the second RT measurement (similar to that illustrated in Figure 19 of reference 9). The differences between the two RT measurements, before and after the HT measurement, are within the dot-to-dot variations observed on dry oxide samples.

A final set of relations used for data analysis are simple modifications of those developed by DiMaria for photo I-V characteristic shift measurements (2,14):

$$N = \frac{1}{e} C_{ox}(\Delta V_p^+ - \Delta V_p^-) = \int_{0'}^{d'_{ox}} \rho(x)dx = -\frac{1}{e} Q \qquad (9)$$

where Q is defined in Equation (2), and

$$\bar{x} = (1 - \frac{\Delta V_p^-}{\Delta V_p^+})^{-1} \cdot d_{ox} = \frac{1}{Q} \int_{0'}^{d'_{ox}} x\rho(x)dx \ . \qquad (10)$$

The above equations are for negative charge trapping. Note that $Q_{ot} = -eN\bar{x}$. These relations are also discussed in the review article by Young (3).

We note explicitly that results quoted below for the densities and cross sections of the dominant trapping centers in dry and water-diffused oxides are a summary of data obtained by the several methods just described. Within the overall error and reproducibility of the several methods, $\Delta V_{FB}(RT)$, $\Delta V_{FB}(HT)$ and ΔV_A measurements yielded internally consistent results. Cross sections were determined using a variation of avalanche current density I_A/A in excess of an order of magnitude.

III. EXPERIMENTAL RESULTS

The overall phenomenon to be examined is indicated very clearly in Figure 8. These data, from a water diffused oxide approximately 500 Å thick, indicate a large negative oxide charge buildup caused by trapping centers with a capture cross section $\sigma_c \sim 10^{-17} cm^2$, and a centroid-weighted areal density Q_{ot} in excess of 3×10^{-7} C-cm^{-2} ($N_{ot} > 2 \times 10^{12} cm^{-2}$). The data also indicate a trapping center with $\sigma_c \sim 10^{-19} cm^2$ and $Q_{ot} \sim 2 \times 10^{-7}$C-cm^{-2} ($1 \times 10^{12} cm^{-2}$). In between these two trap-dominated regimes, an anomalous positive charge Q_{it} in excess of 2×10^{-7}C-cm^{-2} is produced with an effective cross section $\sigma_{eff} = e(\Delta F_A)^{-1} \sim 10^{-18} cm^2$. ΔF_A is the interval of current fluence over which Q_{it} varies significantly, and is defined relative to the injected electron current flux $J_A = F_A/t_A$ (see Table 1).

The same sequence occurs in dry control oxides, with an expanded time scale (i.e., larger ΔF_A values, by approximately one order of magnitude). This is illustrated in Figures 2 and 3. Thus, the dominant trapping center in dry oxides has $\sigma_c \sim 10^{-18} cm^2$, and the anomalous positive charge is produced with $\sigma_{eff} \sim 10^{-19} cm^2$.

We shall proceed to describe separately (A) trapping in control oxides, (B) trapping in water diffused oxides, and (C) the anomalous positive charge effect in both oxide types.

A. Trapping in Dry Control Oxides

ΔV_{FB}(HT) data show clearly that electron trapping in dry control oxides is not a small effect. This is illustrated in Figure 5. Relative to water containing oxides, however, trapping in dry control oxide samples is slow. Specifically, in the region of low injection current fluence ($F_A < 0.3$C-cm^{-2}), electron capture is approximately an order of magnitude less efficient in

dry oxides. This is illustrated in Figures 1 and 5. Table 3 is a summary of electron trapping centers and anomalous positive interface charge measured in dry control oxides.

The results in Table 3 agree generally with the measurements of Young and coworkers (9,17), over the fluence regime in which these several studies overlap. Systematic differences in the amount and kind of trapping centers with $\sigma_c < 10^{-18} cm^2$ are due to the fact that detailed separation of the several traps of this type (see reference 17) was not executed in the present study.

As noted in Section II above, great care was taken to prepare very dry control oxides for the present study. This accounts for the relatively low level of traps with $\sigma_c \sim 10^{-17} cm^2$, since these traps are associated with water impurities. The highly variable,albeit generally small, density of such traps probably resulted from unintentional water contamination of the oxide films during fabrication and storage. The control samples were stored, under dry ambient conditions, during the water diffusion step for the diffused oxides, as discussed in Section II.

One significant difference between the control oxides used in this study and the oxides studied by Young and coworkers was the thickness dependence of the measured flat band shifts. Young and coworkers demonstrated that $\Delta V_{FB} \propto d_{ox}^2$ for dry oxide samples subjected to postmetallization annealing treatments (9). This result, and supporting evidence from photo IV measurements, indicated that electron trapping centers were distributed uniformly throughout the oxide layer.

For the dry control oxides used in the present investigation, which were not given postmetallization annealing treatments, $\Delta V_{FB} \propto d_{ox}$ was approximately obeyed. This is illustrated in Figure 9. The trapped charge centroid, determined from photo IV measurements on several 1000 Å thick samples,

was $\bar{x} \sim 0.35\ d_{ox}$. These results indicate that the trapping centers in dry oxide samples not subjected to postmetallization annealing treatments are concentrated in the outer half of the oxide and/or near the solid-solid interfaces, rather than being distributed uniformly throughout the oxide (9).

The effect of postmetallization annealing on dry control oxides is evident in Figure 5. This result is very similar to that previously reported by Young (see Figure 4 of reference 17). The effect of postmetallization annealing and of extended postoxidation annealing in the low-fluence regime is illustrated in more detail in Figure 10. It is clear from these data that the effect of postmetallization annealing is to remove trapping centers with $\sigma_c \sim 10^{-17} cm^2$. Extended postoxidation annealing significantly reduces the negative oxide charge resulting from trapping centers with $\sigma_c \sim 10^{-18} cm^2$.

To summarize, carefully prepared dry thermal oxide films exhibit significant negative oxide trapped charge buildup. Initial capture efficiencies $N_{ot}\sigma_c$ are of the order of 10^{-5}, and total areal trapped electron density N_{ot} can exceed $10^{12} cm^{-2}$ for large injected electron fluences. The initial capture efficiency can be reduced almost two orders of magnitude by annealing treatments. Postmetallization annealing eliminates trapping centers with $\sigma_c \sim 10^{-17} cm^2$, apparently resulting from low temperature moisture contamination. Extended postoxidation annealing (16 hr at 1000°C in dry N_2) eliminates trapping centers with $\sigma_c \sim 10^{-18} cm^2$.

B. Trapping in Water-Diffused Oxides

Trapping effects in very carefully prepared dry oxide films subjected to a postoxidation water diffusion step at a sample temperature of approximately 150°C are shown in Figures 3-5. Analyses of these and similar data indicate that the dominant effect of low temperature water diffusion is the

introduction of a large density of trapping centers with $\sigma_c \sim 10^{-17} cm^2$. Nicollian and coworkers (5) determined a value $\sigma_c = 1.5 \times 10^{-17} cm^2$ at room temperature. In the present study, measurements at 100°C produced a value $\sigma_c = (1.0 \pm 0.2) \times 10^{-17} cm^2$, in agreement with Young's results on nominally dry oxides without postmetallization anneal (17). It is not clear that this difference is significant, and hence it cannot be interpreted as a variation of σ_c with temperature.

There are also subtle quantitative differences between dry control oxides and water diffused oxides in the density and cross sections of traps with $\sigma_c < 10^{-18} cm^2$. Qualitatively, the electron trapping behavior is similar at fluences $F_A > 0.2$ C-cm^{-2}, as indicated in Figure 5. We shall not address this question further, and shall concentrate on the water related trap with $\sigma_c \sim 10^{-17} cm^2$.

Table 4 is a summary of negative oxide trapped charge associated with electron trapping at this center, and of the anomalous positive interface charge, measured in water-diffused oxides. The saturation value of Q_{ot} exhibits a relatively weak dependence on P_{H_2O}, the water content of the diffusion ambient, as illustrated in Figure 4. There is also a weak dependence on d_{ox}, the oxide thickness, as illustrated in Figure 11. From Figure 11, $\Delta V_p^+ \propto d_{ox}$, so that $Q_{ot} \propto \Delta V_p^+ / d_{ox}$ is independent of the oxide thickness. This is illustrated in more detail in Figures 12 and 13. Using the data of Figures 12 and Equations 9 and 10, the total density N and the centroid $\bar{x}$ of the saturated negative trapped charge can be calculated. Results of these calculations are presented in Figure 14.

The solid lines in Figures 12-14 are least-square best fits of simple polynomials to the data of Figures 12 and 13. For d_{ox} in Angstroms, the

zeroth and first moments of the trapping center distribution are given by

$$N \sim (5\times10^{12} + 2\times10^{9}\ d_{ox})cm^{-2} \qquad (11)$$

and

$$\bar{x} \sim 0.5\ d_{ox}[1 + \frac{d_{ox}}{2000}]^{-1} \qquad (12)$$

These relations hold for diffusion at 150°C for 10 minutes, with $P_{H_2O} \sim 50$ mm Hg.

Measurements for P_{H_2O} = (30-150)mm Hg are similar to those just described. For this diffusion regime, in which the anomalous positive charge effect is large (see Figure 8), the distribution of water-related trapping centers does not depend strongly on the water content of the diffusing ambient.

Equation 12 contains a length parameter approximately equal to 2000 Å. This can be interpreted as a characteristic diffusion length or penetration depth D for the water-related trapping centers. For the diffusion conditions studied, we might expect that in films with $d_{ox} << D$, $\bar{x} \sim 0.5\ d_{ox}$ and $N \propto d_{ox}$. For this case, the trapping centers would be uniformly distributed throughout the oxide and $\Delta V_{FB} \propto \bar{x}N \propto d_{ox}^{2}$.

In the other extreme, we might expect that for $d_{ox} >> D$, $\bar{x} \sim 0.5\ D$ and N would be independent of d_{ox}. For this case, the trapping center distribution would not penetrate the oxide layer and $\Delta V_{FB} \propto \bar{x}N$ would be independent of d_{ox}.

Both of these cases have been demonstrated. Figure 15 shows the result of postoxidation water diffusion at a sample temperature of 300°C, which should have the effect of greatly increasing the water diffusion depth D. Figure 16 shows the same data replotted, indicating that $\Delta V_{FB} \propto d_{ox}^{2}$, as expected for $D > d_{ox}$. Photo IV data on these samples are consistent with these data, showing that $\bar{x} \sim 0.5\ d_{ox}$.

In the other extreme, Figure 17 shows the result of postoxidation water diffusion at a sample temperature of 135 °C. For samples with $d_{ox} > 1500$ Å, ΔV_{FB} is approximately constant (i.e., independent of d_{ox}). This is consistent with the conditions $D < d_{ox}$, and with photo IV data indicating that the centroid of the oxide trapped charge distribution is located away from the center of the film and toward the Al-SiO_2 interface.

These conclusions are qualitatively consistent with the water diffusion model proposed by Nicollian, et al., for generation of the water-related electron trapping centers (5). However, the penetration depth determined by the analysis described above ($D \sim 2000$ Å for a diffusion temperature of 150°C) is much larger than the characteristic diffusion length ($\sim$500 Å) determined by Nicollian, et al., from etch-back profiling of oxide trapped charge. The larger depth is in fact more consistent with the qualitative description presented by these authors (5,6) of conditions under which water does not penetrate to the Si-SiO_2 interface.

Figure 18 shows data obtained at a fixed avalanche-injected charge fluence on thick oxides subjected to postoxidation water diffusion at 135°C. These data indicate that ΔV_{FB} is approximately proportional to $\sqrt{P_{H_2O}}$ in the regime in which $D < d_{ox}$. This is not consistent with results reported by Nicollian, et al. (5). Note, however, that this dependence was not observed for $d_{ox} \sim 1000$ Å and $T_{DIFFUSION} \sim 150$°C in the present study, as discussed above. For these latter conditions, it is reasonable to assume that $D \sim d_{ox}$, and that the water-related trapping center distribution is complicated by the presence of a diffusion barrier (the Si surface) and possibly by solubility limitations at the SiO_2 surface. On this last point, the data in Figures 14 and 16 indicate that average volume trap densities $N\, d_{ox}^{-1}$ are of the order of $10^{18}\,cm^{-3}$. This is much less than

water species concentrations observed in thermal oxide films grown in water containing environments (18,19).

To summarize, the effect of water indiffusion on very dry thermal oxide films is the introduction of an electron trapping center with $\sigma_c \sim 10^{-17} cm^2$. The distribution of these trapping centers is characterized by an effective length D. D is approximately 2000 Å for a diffusion temperature of 150°C, and is approximately 1300 Å (see Figure 17) for a diffusion temperature of 135°C. In the limit $d_{ox} > D$, the saturated negative oxide trapped charge produced by electron capture at the water-related trapping centers obeys the relation

$$Q_{ot} \propto \sqrt{P_{H_2O}} , \qquad (13)$$

where P_{H_2O} is the water content of the diffusing ambient. In the limit $d_{ox} << D$, the trapping centers are distributed uniformly in the oxide layer, with a volume density of approximately $10^{18} cm^{-3}$.

3. Anomalous Positive Charge

Anomalous positive charge Q_{it} or N_{it} is employed here in a modified sense from the definition given by Deal (16). Young and coworkers (9) and Miura and coworkers (11) have demonstrated that at least a major fraction of measured positive charge generated by avalanche injection of electrons is interface trapped charge in the strict sense of Deal. That is, the positive charge measured under flat band conditions is due to ionized donor-like states at the $Si-SiO_2$ interface in thermal and electrical communication with the Si surface. This point was not addressed systematically in the present study, although Lai (20) has shown in one of the

present samples that ionized donor-like states accounted for a major fraction of Q_{it}. They did not account for all of Q_{it}. These results for D_{it}, the interface trapped charge state density, are shown in Figure 19. These data were obtained by comparison of high frequency C-V and linear ramp I-V measurements (21).

Thus, in fact, anomalous positive charge Q_{it} consists primarily of ionized donor-like states. There is some admixture of fixed positive charge, located spatially within 50 Å of the $Si-SiO_2$ interface and energetically away from the Si band gap (16). Q_{it} is measured, according to the prescriptions of Equations 7A-C, as the difference in the displacement of the room temperature flat band voltage shift and the displacement in voltage of other MOS device characteristic curves which are insensitive to interfacial charge and states. Thus, Q_{it} is a convenient and reproducible, but arbitrary, measure of the net change in oxide fixed charge and interface trapped charge produced by avalanche injection and transport of an electron current in the oxide.

As indicated in Figures 2 and 3, the room temperature flat band shift reversal produced by anomalous positive charge buildup at the $Si-SiO_2$ interface occurs in both dry control oxides and water diffused oxides. Tables 3 and 4 contain summary data for dry and wet oxides, respectively. In both types of films, the magnitude of the positive interface charge density Q_{it} was approximately equal to the magnitude of Q_{ot}, the centroid-weighted negative oxide trapped charge density associated with the dominant and most efficient electron trapping center. Also, anomalous positive charge buildup occurred over a definite and finite time regime in both types of films, as indicated in Figure 8 for water diffused oxides.

Two additional characteristics of the flat band reversal phenomenon are illustrated in Figures 20-22 for water diffused oxide films. First, it was approximately true that the avalanche injection charging curve (ΔV_{FB} vs t_A) scaled with the avalanche charge fluence F_A. Figure 20 exhibits $\Delta V_{FB}(RT)$ vs. t_A for several different currents I_A, and Figure 21 exhibits the same $\Delta V_{FB}(RT)$ data replotted as a function of F_A. Deviations of the several data plots in Figure 21 from a single renormalized curve indicate a flux dependence of the effective cross section σ_{eff} for positive charge generations. Miura and coworkers (22) have recently discussed a charge flux (i.e., current density) dependence of interface state generation. We shall consider below only the first order effect, the general variation of Q_{it} with F_A, neglecting the current density dependence (20). Second, Figure 22 indicates that positive charge generation was only weakly dependent on the water content of the diffusing ambient. This statement applies in the diffusion regime in which, as discussed above, the effective water diffusion depth $D \gtrsim d_{ox}$.

Figures 23-26 indicate the detailed variation of Q_{it} with avalanche charge fluence F_A. In these figures, the curves marked "Q_{ot}" were obtained from ΔV_{FB} data measured at 100°C (see Equation 4, and Figures 2, 3, and 5). The curves marked "$Q_{ot} + Q_{it}$" were also obtained directly from experimental data, ΔV_{FB} measured at 22°C (see Equation 3, and Figures 2 and 3). The curve marked "Q_{it}" was calculated by subtracting the two experimental curves (see Equation 7A).

In all cases, the Q_{it} vs. F_A curves have the general appearance of simple first order kinetic variations, i.e., Q_{it} an exponentially increasing function of F_A, with two modifications. First, the initial linear portion

of the several curves persists over too long a fluence interval, compared to a true exponential behavior. Basically, the initial increase of Q_{it} is too slow. Second, there is in Figures 24-26 a slow linear decrease in Q_{it} at large fluence values. We will not presently address this phenomenon.

Figure 27 indicates clearly the qualitative description just stated. Figure 27 was obtained from the Q_{it} vs. F_A curves by the following procedure. First, the linear decrease at large F_A values is extrapolated to $F_A = 0$ and added to the Q_{it} curves in Figures 23-26. This produces a modified Q_{it} vs. F_A curve which is asymptotic to a zero-slope line with intercept Q_M. Q_M is thus the saturated steady state value of Q_{it} which would have been reached in the absence of the unexplained linear decrease. Second, the quantity $(Q_M-Q_{it}) \div Q_M$ is calculated, using the modified Q_{it} values. Finally, $(Q_M-Q_{it}) \div Q_M$ is plotted against F_A, on a semilogarithmic scale (Figure 27).

The results summarized in Figure 27 indicate that Q_{it} increases exponentially with F_A at large fluences, in both wet and dry oxides. Thus

$$Q_{it} \sim Q_M \{1-\exp[-\frac{1}{e} \sigma_{eff} \cdot (F_A-F_0)\} \text{ for } F_A > 2F_0 \qquad (15)$$

where σ_{eff}, the effective cross section for interface positive charge generation can now be precisely defined, and F_o is in effect an initial time delay. For $F_A < 2F_o$, the increase in Q_{it} is approximately linear, rather than exponential. Table 5 exhibits values of σ_{eff} and F_o for the two oxide types.

The observed behavior of the anomalous positive charge, summarized in Figure 27 and Equation 15, indicates that generation of this charge requires at least two steps initiated by the avalanche injected electron flux.

First, it appears that positive charge buildup can only occur subsequent to the production of negative oxide trapped charge. We suggest that this accounts for the initial delay F_o in the approach to simple first order kinetic behavior (see Equation 15). We suggest specifically that some defect configuration formed in the bulk of the oxide film during or subsequent to electron capture and localization at trapping centers in the film is a precursor for the defect or impurity structure responsible for the donor state distribution exhibited in Figure 19. This statement presumably also applies to any defect/impurity structure that results in a fixed oxide charge component of positive Q_{it}, as discussed above.

In the simplest case, the trapped electron center itself would be the precursor of the interface donor-state center and the positive fixed-charge center. For this case, the following kinetic equations would apply:

$$\frac{dN_{ot}(F_A)}{dF_A} = + \frac{\sigma_c}{e}\{N_{ot}(\infty)-N_{ot}(F_A)\} \tag{16}$$

$$\frac{dN_{it}(F_A)}{dF_A} = + \frac{\sigma_{eff}}{e}\{N_{ot}(F_A)-N_{it}(F_A)\} \tag{17}$$

Thus, for $F_A < e\sigma_c^{-1}$, the amount of negative oxide charge Q_{ot} controls the production of Q_{it}. For $F_A >> e\sigma_c^{-1}$, Q_{ot} has attained its saturated value $Q_{ot}(\infty)$, and Q_{it} would be expected to obey the relation

$$Q_{it}(F_A) \sim Q_{ot}(\infty)\{1-\exp[\frac{\sigma_{eff}}{\sigma_c} - \frac{1}{e}\sigma_{eff} F_A]\} \tag{18}$$

This last equation is heuristic. In general, the exponent term σ_{eff}/σ_c might be weighted by a numerical factor of order unity. Comparison of Equation 15 with Equation 18 shows that this simple model requires that

$Q_{it}(\infty) = Q_M \gtrsim Q_{ot}(\infty)$ and that the delay period $F_o \lesssim e\sigma_c^{-1}$. Examination of the calculated results for Q_{it} in Table 5, and comparison with Q_{ot} results for dry oxides (Table 3) and water diffused oxides (Table 4) show that these conditions are approximately fulfilled. The calculated values of F_o are somewhat less than $e\sigma_c^{-1}$ if σ_c is the capture cross section of the dominant trap in each oxide.

A second step required for formation of anomalous positive charge is also initiated in some way by the injected electron flux I_A/A. This process is characterized by the effective cross section σ_{eff}. It is not known from the present work whether this step occurs within the oxide bulk or at the $Si-SiO_2$ interface. It is clear, however, that the model just presented does require transport of some quantity (mass or energy or both) from the bulk of the oxide, where Q_{ot} is located, to the interface region, within which Q_{it} is measured. This transport could obviously occur after the first kinetic step described above (electron trapping in the oxide bulk) or after the second kinetic step (which results in interface donor state generation and/or positive fixed charge localization at the interface).

To summarize, anomalous positive charge generation occurs in both dry control oxides and water diffused oxides. This positive charge, measured under flatband conditions, involves both interface trapped charge (donor-like states) and oxide fixed charge contributions. In both types of oxides, the amount of positive interface charge and the early-stage generation kinetics of this charge are determined by the dominant occupied electron trapping center in the bulk of the oxide film. We suggest that the occupied electron trap responsible for negative Q_{ot} is a direct or indirect precursor for the interface defect responsible for positive Q_{it}.

In addition to the precursor formation, the avalanche injected electron flux is apparently required to initiate a second kinetic step necessary to final formation of Q_{it}. The effective cross section for this second process differs for dry control oxides and water diffused oxides.

Finally, within the framework of the model proposed, transport of energy and/or mass from the oxide bulk to the semiconductor oxide interface must occur at some point in the overall kinetic process resulting in Q_{it}.

We emphasize that the results just described, particularly the behavior of the anomalous positive charge associated with fast and slow interface states and fixed oxide charge, pertain to the specific set of sample fabrication conditions described in Section II. It is very clear that these effects are extremely sensitive to details of both the oxidation procedure and any post oxidation sample treatments (including storage conditions). Individual samples have been prepared in which the anomalous positive charge effect dominated electron trapping (so that ΔV_{FB} was negative from $t_A \sim 0$) and in which the magnitude of Q_{it} was much less than the magnitude of Q_{ot}. The effects of annealing treatments are well characterized (see Fig. 10 and ref. 17). It was also clear in our program that extended storage of dry oxides in nominally dry ambients produced effects similar to water in-diffusion, even if the oxide had been covered with a thin ($\sim$15 nm) Al electrode. The effect of other processing variations, however, is not well understood.

IV. DISCUSSION AND CONCLUSIONS

Diffusion of water into dry thermal oxide films results in the formation of an impurity related center which is responsible for electron trapping in the bulk of the oxide film, and also for generation of donor-like states and fixed positive charge in the vicinity of the $Si-SiO_2$ interface. It is clear that some defect structure which produces the same general response to an injected electron flux also exists in very dry thermal oxide films. The dramatic difference between the two types of films in negative oxide charge buildup and anomalous positive charge generation at low injected electron fluences is illustrated in Figure 1. The results summarized in Tables 3 and 4, and in Figure 5, indicate that this difference is not primarily due to differences in trapping center densities, but rather to the specific properties of the dominant electrically active defect in each film.

A. Trapping in Dry and Water Diffused Oxides

In both dry and water diffused oxides, the capture cross section of the dominant electron trapping center is smaller than that anticipated for a simple electrically neutral defect. For a simple neutral defect, the capture radius $r_c = \sqrt{\sigma_c/\pi}$ should be an atomic radius ($r_c > 0.5$ Å). In fact, for dry oxides $r_c \sim 0.05$ Å, and for water diffused oxides $r_c \sim 0.2$ Å. A general explanation for such small cross sections is modulation of a neutral trapping center (with a square well core potential having a capture cross section 10^{-16}-10^{-14} cm^2)(4) by some effective probability factor. Specific examples include situations in which only conduction electrons with sufficient kinetic energy to overcome a repulsive potential barrier are captured (2) or in which capture into a long-lived shallow excited state is unstable against thermal excitation. In the context of this model, the primary effect of

water indiffusion is to increase the core diameter and/or reduce the probability factor.

The most economical assumption is that water indiffusion has the net effect of dressing existing neutral defects in dry oxide films. It is not possible at present to specify detailed models for these trapping centers. Several distinct possibilities exist for the overall mechanism, however. First, fragments of the diffusing water molecules may be bonded into structural defects in the SiO_2 network. Triply-bonded Si or peroxy radicals, for example, have been identified by EPR studies in bulk glasses. In an ionic bookkeeeping scheme, the two defects just mentioned correspond to oxygen vacancies and oxygen interstitials, respectively. Characterization of the properties of very dry, and presumably very clean, oxides in terms of such intrinsic defects is reasonable. Dressing of such defects by water fragments would produce Si-H and Si-OH ligand complexes. There is firm experimental evidence for such ligands (23). The major difficulty with this scheme is the absence of any convincing evidence, from bulk silica studies, that either the bare intrinsic defects or the dressed defects trap single electrons. Note that this is not decisive evidence against such a mechanism in the present case, since bulk trapping studies invariably involved two-carrier generation (electron-hole pairs produced by ionizing radiation) rather than single carrier transport.

A second model for the effect of water indiffusion is ion exchange. If, for example, the dry oxide films contained trapping centers involving non-mobile Na impurities, the effect of water diffusion could be to replace the Na impurities with H-impurities. This mechanism certainly occurs in bulk glasses at higher temperatures than those employed in the diffusion steps in the present program (24).

The suggestion that Na replacement by H is the important result of water diffusion clearly implies that a significant concentration of non-mobile Na exists in the dry control oxides. Since the amount of non-mobile Na required to account for trapping center concentrations observed in the present study is relatively high (average volume concentration $Q_{ot}/\bar{X}$ in excess of $5x10^{17}cm^{-3}$), this seems unlikely. What has in fact been demonstrated, however, is that the concentration of mobile Na in our films is at least two orders of magnitude less than the saturated concentration of $Q_{ot}/\bar{X}$. The presence of sufficient non-mobile Na to account for dry oxide trapping has not been definitively ruled out. Thus, an ion exchange process of trapping center modification by water fragments has not, at this point, been definitively eliminated.

A third model for the effect of water indiffusion, consistent with the trapping results, is simple association (i.e.,proximity) of a water related ligand complex (involving Si-H or Si-OH bonds),or of dissolved molecular H_2O,with some dry oxide trapping center involving an intrinsic structural defect or an impurity related defect. Very recently, Hartstein (23) has demonstrated that water indiffusion increases significantly the SiOH concentration, and that this can be subsequently reduced by postmetallization annealing. Thus, the SiOH content varies with sample treatment (water diffusion and PMA) in a way that parallels the variation of σ_c for the dominant electron trapping center.

We note explicitly that the proximity model addresses one problem cited above, namely that the SiOH ligand structure and any intrinsic precursor defect in a dry oxide have not been demonstrated to be electron trapping centers. It does not address the more general problem, namely

that either some intrinsic defect which does trap electrons must exist in the clean, dry oxides, or that a relatively large concentration of some impurity must exist in these oxides. Present data require approximately 50 of one or the other defect per million SiO_2 molecules.

B. Positive Interface Charge Generation

The model proposed in Section IIIC does not invoke any special preparation of the Si-SiO_2 interface as a requirement for anomalous positive charge generation. Dry oxide films exhibit a large positive charge anomaly, differing from that observed in water diffused oxides primarily in the overall efficiency of the process. Therefore, it does not seem necessary to assume that prior modification of the interface by water-related impurities is necessary to the generation of interface charge, as suggested by Nicollian and coworkers (5).

The most important problem that arises in connection with the model proposed in Section IIIC is the identity of the species which diffuses from the oxide bulk to the Si-SiO_2 interface. Weinberg and coworkers have considered this problem in some detail, within a more general context (25). The two possible diffusing species suggested by these authors -- a water fragment (most likely neutral atomic hydrogen) or an exciton -- are consistent with the present result.

Nicollian and coworkers (5) reported evidence for release of hydrogen during the electron capture process. It was not possible to demonstrate a quantitative correlation between the released hydrogen and the oxide trapped charge, however. In the present model, hydrogen release could be correlated with the second kinetic step, occurring subsequent to electron capture.

If atomic hydrogen diffuses to the interface during generation of positive interface charge, then the electron trapping center in dry oxides must involve hydrogen impurities. There is experimental evidence that measurable concentrations of water-related species exist in the dry oxide films, even though these films were prepared in oxidants containing less than 1 ppm H_2O (23). It is not clear, however, that these concentrations are sufficient to account for Q_{ot} ($\sim 5 \times 10^{17} cm^{-3}$ average volume concentration).

On the other hand, excitons may be the species which diffuses to the interface (25). The model proposed above then requires that these excitons are produced via an interaction between the conduction electrons and a negatively-charged trapped electron center, which interaction does not change the net charge of the center. This process would have to be an Auger excitation involving some small fraction of the avalanche-injected conduction electrons which are quite hot under the SiO_2 internal field conditions prevailing in our experiments ($\gtrsim 10^6$ V-cm^{-1}). DiMaria, et al., have reported hot electron effects under generally similar conditions (26), with generally similar efficiencies ($\sim 10^{-6}$). These electrons were produced by internal photoemission, rather than avalanche injection.

C. Kinetics of Water Diffusion

Qualitatively, the buildup of Q_{ot} in water diffused oxides studied in the present investigation was similar to that reported by Nicollian, et al. (5). There are, however, some rather significant quantitative differences. If, as all investigators have assumed, the spatial distribution of electron trapping centers with $\sigma_c \sim 10^{-17} cm^2$ is determined by low temperature water diffusion, then the parameter D can be interpreted in terms of a characteristic diffusion length x_o. Using the model described by Nicollian, et al.,

we obtain $x_o \sim D/3 \sim 600$ Å for a ten minute diffusion at 150°C. Nicollian, et al., obtained $x_o \lesssim 200$ Å. In addition, Nicollian, et al., reported $\Delta V_{FB} \propto P_{H_2O}$, whereas we obtain $\Delta V_{FB} \propto \sqrt{P_{H_2O}}$ for $d_{ox} > D$, and ΔV_{FB} approximately independent of P_{H_2O} for $d_{ox} \lesssim D$.

We have no explanation for these differences. The basic oxidation process was different in the two studies. The Bell Laboratory oxides were grown under a negative electric stress, a procedure presumed to restrict monovalent impurities to the oxide surface (27).

D. Conclusions

All things considered, negative oxide trapped charge formation in dry oxides is most plausibly attributed to an intrinsic or H/OH compensated structural defect grown into the amorphous SiO_2 network at high temperatures. This defect can be dressed by fragments of water molecules incorporated in the oxide layer at low temperatures. This latter process increases the capture cross section of the neutral trapping center by an order of magnitude, and enhances the efficiency of the negatively-charged captured electron center in generating a mobile hydrogen atom or an exciton via an interaction with mobile electrons. Transport of the resultant mobile species (a water molecule fragment or an exciton) to the $Si-SiO_2$ interface results in formation of interface positive charge. The detailed reaction at the interface, and the complete structure of the charged interface defect, is not known.

The overall process of positive interface charge (Q_{it}) generation during injected electron transport is somewhat analogous to mobile ionic charge (Q_m)generation (16). The obvious difference is the source location and release mechanism of the mobile species which migrates to the $Si-SiO_2$ interface. In the case of Q_m, the mobile species is an Na^+ ion thermally

released from the Al-SiO_2 interface region. In the case of Q_{it}, the mobile species is electrically neutral in general (25), and is released by inelastic electron scattering from trapped electron centers distributed throughout the SiO_2 bulk. As noted above, we have not definitely disproved the possibility that, in the present case, "non-mobile" Na bonded into the dry oxide electron traps is the mobile species responsible for Q_{it} generation. The number of impurities required, and the neutral character of the mobile species in other situations, make this an unlikely possibility, however. Also, the effect of an applied bias at elevated temperatures, as described by Young and coworkers (9) and verified in the present program, is to produce a flat band shift ΔV_{FB} opposite to that expected for mobile ionic charge. Q_{it} buildup cannot therefore be related to any mechanism involving release of Na^+.

An exciton mechanism for Q_{it} generation does not require 50 parts per million impurity concentrations in the dry, and presumably clean, control oxide. In this case, intrinsic defects in the silica network could be responsible for electron trapping and Q_{ot} formation. However, the exciton model does require an Auger-like transition involving some hot fraction of the injected conduction electron distribution. Clearly, independent verification of such a process is required.

Finally, we note that the proposed exciton process is not self limiting, unless the excitation also produces a permanent change in some configuration coordinate. Thus, a given trapped electron center could produce an indefinite number of excitons. Q_{it} generation would thus have to be limited in some other manner, such as a fixed number of available interface defects at which donor-like states or fixed positive charge can be formed.

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Table 1

Characteristic Fluence Intervals

$\sigma_c = e \cdot \Delta F_A^{-1}$ where $Q(\Delta F_A) = 0.5\ Q_{MAX}$

σ_c (cm^2)	ΔF_A ($C\text{-}cm^{-2}$)
10^{-17}	0.01
10^{-18}	0.1
10^{-19}	1

Table 2

Dependence of Oxide Trapped Charge on H_2O Diffusion

ΔV_{FB}, $\Delta V_p{}^+$, ΔV_a Comparison

SAMPLE $T_{DIFFUSION}$=150°C $t_{DIFFUSION}$=10 min	INJECTION FLUENCE (C-cm^{-2})	ΔV_{FB} (V)	$\Delta V_p{}^+$ (V)	ΔV_A (V)	ERROR (V)
Control (1000 Å)	0.18	2.4	2.6	2.9	± 0.5 V
P_{H_2O}=52 mm Hg (1000 Å)	0.035	6.0	10.2	9.3	± 0.7 V
	0.18	0.5	8.3	8.0	± 1.0 V
P_{H_2O}=103 mm Hg (1000 Å)	0.027	7.3	12.3	8.9	± 1.5 V
	0.12	1.4	12.5	10.0	± 1.0 V
P_{H_2O}=149 mm Hg (1000 Å)	0.038	5.5	11.8	12.5	± 0.75 V
	0.18	1.0	11.9	10.5	± 1.0 V

Table 3

DRY OXIDE CONTROL SAMPLES

T_{ox} = 1000°C	d_{ox} = (540-1620) Å
POA = 1000°C, 1h, N_2	NO PMA

NEGATIVE TRAPPED CHARGE

$\sigma_c(cm^2)$	$N_{ot}(cm^{-2})$
$(1\text{-}4) \times 10^{-18}$	$(5\text{-}15) \times 10^{11}$
$(2\text{-}3) \times 10^{-19}$	$\sim 10 \times 10^{11}$
$(1\text{-}3) \times 10^{-17}$	$(0.1\text{-}1) \times 10^{11}$

POSITIVE INTERFACE CHARGE

σ_{eff} (cm^2)	N_{it} (cm^{-2})
$(5\text{-}10) \times 10^{-19}$	$\sim 20 \times 10^{11}$

Table 4

DIFFUSED OXIDE MOS SAMPLES

T_{ox} = 1000°C d_{ox} = 1025 Å

POA = 1000°C, 1h, N_2 NO PMA

DIFFUSION: $T_{DIFFUSION}$ = 150°C, $t_{DIFFUSION}$ = 10 min

P_{H_2O} ~ 50 - 150 mm Hg

P_{H_2O} (mm Hg)	N_{ot} (cm^{-2})	N_{it} (cm^{-2})
	F_A = 0.033 C-cm^{-2} = 2 × 10^{17} e/cm^2	
52	2.2 × 10^{12}	0.9 × 10^{12}
102	2.6 × 10^{12}	1.1 × 10^{12}
148	2.5 × 10^{12}	1.3 × 10^{12}
	F_A = 0.16 C-cm^{-2} = 1 × 10^{18} e/cm^2	
52	1.9 × 10^{12}	1.6 × 10^{12}
102	2.7 × 10^{12}	2.3 × 10^{12}
148	2.5 × 10^{12}	2.3 × 10^{12}

Table 5

Kinetic Parameters for Positive Interface Charge Generation

SAMPLE	e/F_o (cm^2)	σ_{eff} (cm^2)
Dry Control, no PMA	8.5×10^{-19}	1.1×10^{-18}
Dry Control, PMA	4.8×10^{-19}	1.0×10^{-18}
Water Diffused (P_{H_2O} - 30 mm Hg)	2.8×10^{-18}	2.1×10^{-18}
Water Diffused (P_{H_2O} - 50 mm Hg)	5.6×10^{-18}	2.2×10^{-18}

FIGURE CAPTIONS

FIG. 1. Flat band voltage shifts resulting from avalanche injection of electrons into a dry control oxide and a water diffused oxide. These data span the low fluence regime.

FIG. 2. Flat band voltage shifts resulting from avalanche injection of electrons into a dry control oxide, measured at room temperature and at 100°C.

FIG. 3. Flat band voltage shifts resulting from avalanche injection of electrons into a water diffused oxide, measured at room temperature and 100°C.

FIG. 4. MOS device characteristic shifts measured on a dry control oxide and two water diffused oxides. All data were obtained at room temperature. The solid squares are C-V flatband shifts ΔV_{FB}, the solid circles are avalanche control voltage shifts ΔV_A at constant current, and the crosses are photo I-V voltage displacements ΔV_p^+. Solid lines are for visualization convenience only.

FIG. 5. MOS device charging curves Q_{ot} vs. F_A, measured at 100°C. Data are shown for two different dry control oxides (PMA and no PMA), and one water diffused oxide (no PMA).

FIG. 6. Flat band voltage shifts resulting from avalanche injection of electrons into a water diffused oxide, measured at 22°C and 100°C. These data were obtained in the very low fluence regime.

FIG. 7. Flat band voltage shifts resulting from avalanche injection of electrons into a water diffused oxide, measured at 22°C and 100°C. The two room temperature data runs were made before (B) and after (A) extensive wafer treatment at 100°C.

FIG. 8. MOS device charging curve measured on a water diffused oxide. Data were obtained at room temperature.

FIG. 9. MOS device charging curves measured on two dry control oxides. Data were obtained at 100°C. Since $|Q_{ot}| \propto \Delta V_{FB}(HT)/d_{ox}$, coincidence of the two curves would imply that $\Delta V_{FB}(HT) \propto d_{ox}$.

FIG. 10. Flat band voltage shifts resulting from avalanche injection of electrons into a dry control oxide, measured at 120°C. Data are shown for four different annealing conditions, as indicated. Postoxidation annealing (POA) is performed in a dry nitrogen ambient, and postmetallization annealing is performed in a forming gas ambient (PMA).

FIG. 11. MOS device characteristic shifts measured on a water diffused oxide. Diffusion conditions were P_{H_2O} = 52 mm Hg at a temperature of 150°C for 10 minutes. Data are shown for two different oxide thicknesses. Solid lines are for visualization convenience only.

FIG. 12. Photo IV characteristic voltage displacements produced by avalanche injection of electrons into a water diffused oxide. The top figure refers to voltage displacements ΔV_P^+ measured under positive bias, the bottom figure refers to voltage displacements ΔV_P^- measured under negative bias. Data were obtained at room temperature, at an avalanche fluence $F_A \sim 0.2$ C-cm^{-2}.

FIG. 13. Oxide trapped charge characteristics calculated from the data of Fig. 12. The calculations are described in the text.

FIG. 14. Oxide trapped charge characteristics calculated from the data of Fig. 12. The calculations are described in the text.

FIG. 15. Flat band voltage shifts resulting from avalanche injection of electrons into water diffused oxides. All data were measured at 120°C, using an avalanche injected average current density of 60μA-cm^{-2}.

FIG. 16. Normalized flat band voltage shifts resulting from avalanche injection of electrons into water diffused oxides. These data runs are the same as shown in Fig. 15, weighted by the quantity d_{ox}^{-2} and normalized to the data obtained on the sample with $d_{ox} \approx 98$ nm.

FIG. 17. Average flat band voltage shift resulting from avalanche injection of electrons into water diffused oxides. Each data point is the statistical average of a data run similar to those shown in Fig. 15, to a fluence $F_A \sim 0.1$ C-cm^{-2}. All data were obtained at a temperature of 120°C.

FIG. 18. Average flat band voltage shift resulting from avalanche injection of electrons into water diffused oxides. Each data point is a statistical average of a data run similar to those shown in Fig. 15, to a fluence $F_A \sim 0.01$ C-cm^{-2}. All data were obtained at a temperature of 120°C.

FIG. 19. Interface state distribution resulting from avalanche injection of electrons into a water diffused oxide. Data were obtained subsequent to an avalanche injection fluence $F_A \sim 0.2$ C-cm^{-2}, at room temperature.

FIG. 20. Flat band voltage shifts resulting from avalanche injection of electrons into water diffused oxides, measured at 22°C. These data runs were made on different electrodes on a single half-wafer.

FIG. 21. Flat band voltage shifts resulting from avalanche injection of electrons into water diffused oxides. These data runs are the same as those exhibited in Fig. 20, replotted as a function of the avalanche injection electron fluence $F_A = I_A \cdot t_A$.

FIG. 22. Flat band voltage shifts resulting from avalanche injection of electrons into water diffused oxides, measured at 22°C. The three different MOS samples were prepared under identical conditions, except for the H_2O partial pressure during separate, but otherwise identical, diffusion steps.

FIG. 23. MOS device charging curves obtained on a dry control oxide which had been given a postmetallization anneal (forming gas ambient at 400°C for thirty minutes). The two lower curves were obtained from data similar to that in Fig. 2. The top curve was calculated (see text).

FIG. 24. MOS device charging curves obtained on a dry control oxide (no PMA). The two lower curves were obtained from data similar to that in Fig. 2. The top curve was calculated (see text).

FIG. 25. MOS device charging curves obtained on a water diffused oxide. The two lower curves were obtained from data similar to that in Fig. 3. The top curve was calculated (see text).

FIG. 26. MOS device charging curves obtained on a water diffused oxide. The two lower curves were obtained from data similar to that in Fig. 3. The top curve was calculated (see text).

FIG. 27. Kinetics of positive interface charge buildup. Construction of this curve from the Q_{it} charging curves in Figs. 23 and 25 is described in the text. The dash lines are exponential functions fitted to the points at larger fluence values.

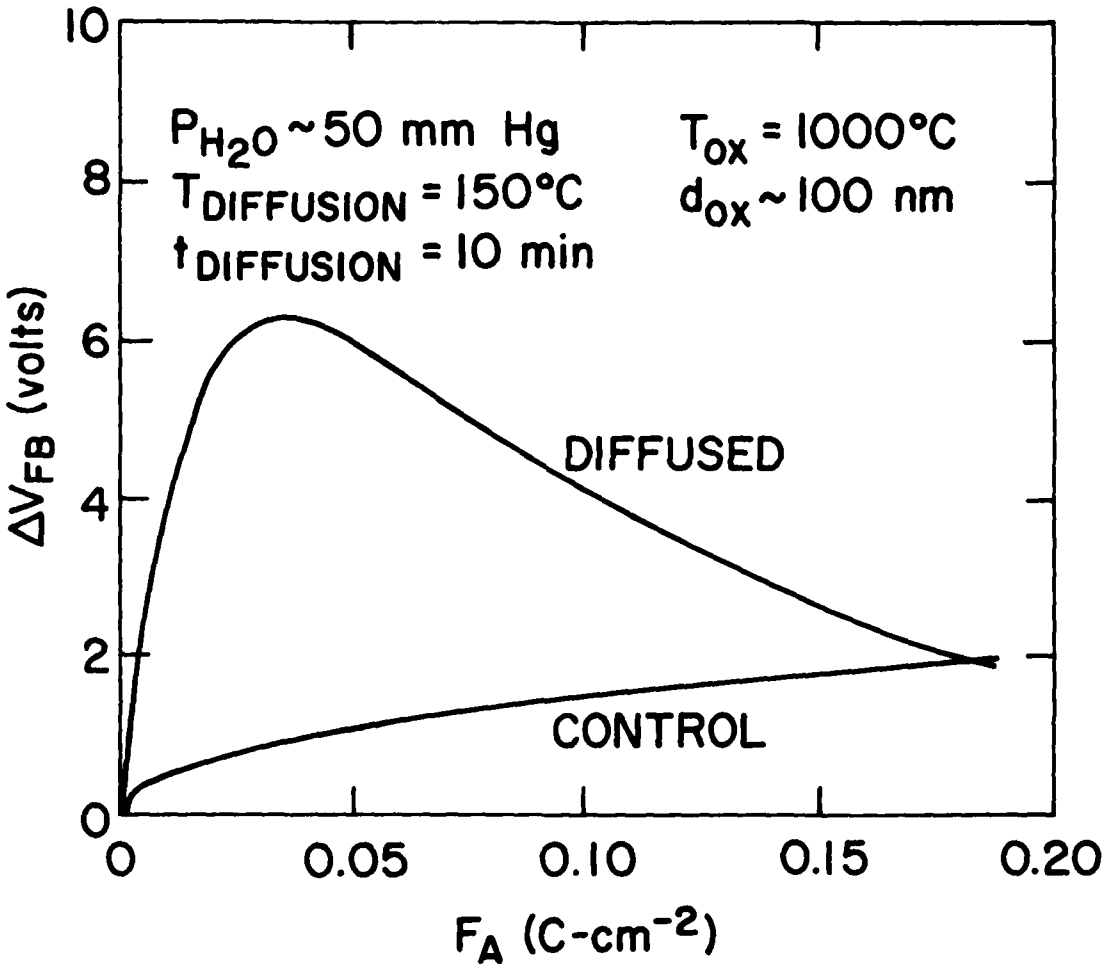

10
8
6
4
2
0
P_{H_2O} ~ 50 mm Hg
$T_{DIFFUSION}$ = 150°C
$t_{DIFFUSION}$ = 10 min
T_{ox} = 1000°C
d_{ox} ~ 100 nm
DIFFUSED
CONTROL
ΔV_{FB} (volts)
0
0.05
0.10
0.15
0.20
F_A (C-cm^{-2})

FIGURE 1

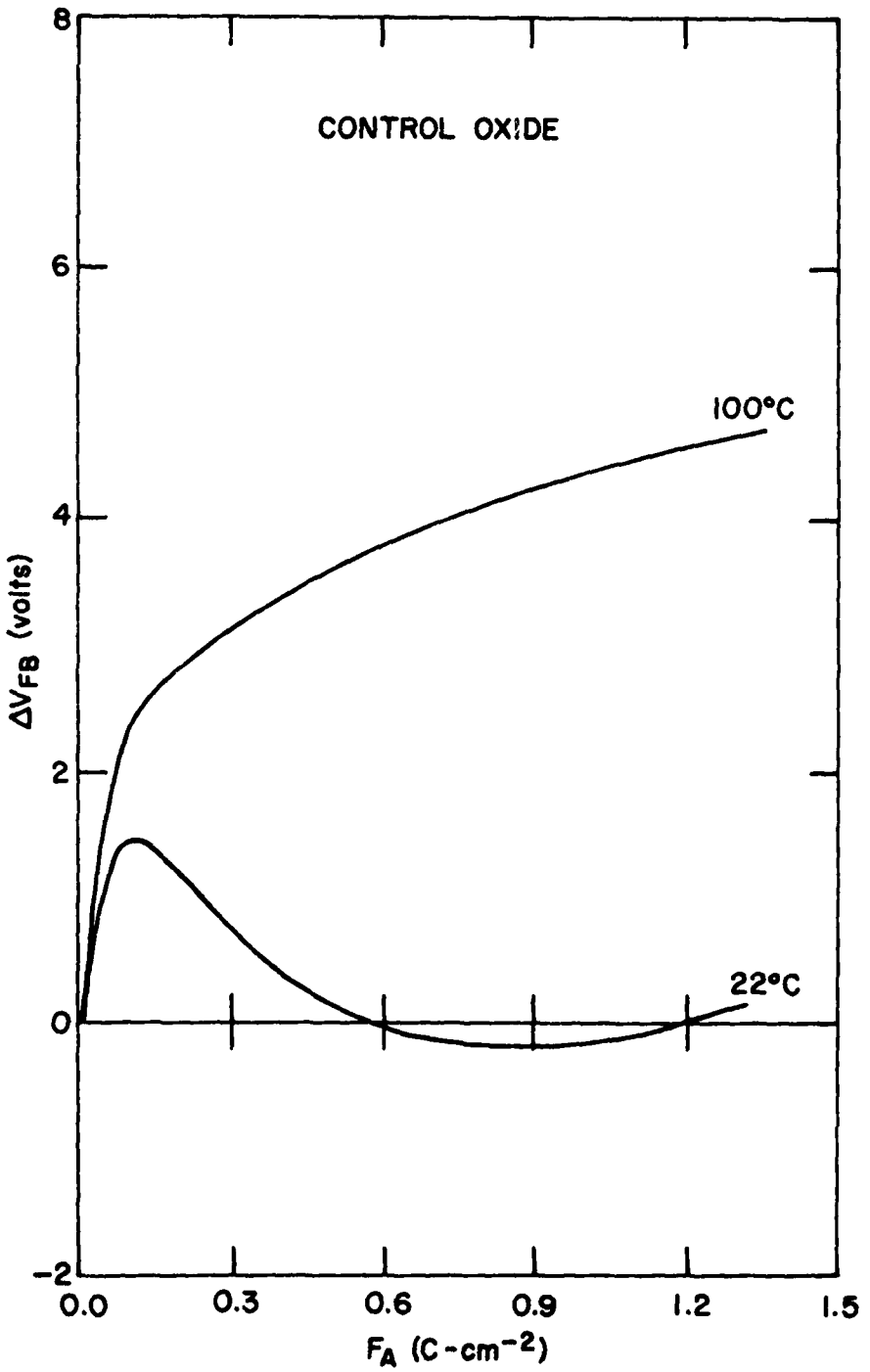

CONTROL OXIDE
100°C
22°C
8
6
4
2
0
-2
0.0
0.3
0.6
0.9
1.2
1.5
ΔVFB (volts)
FA (C-cm-2)

FIGURE 2

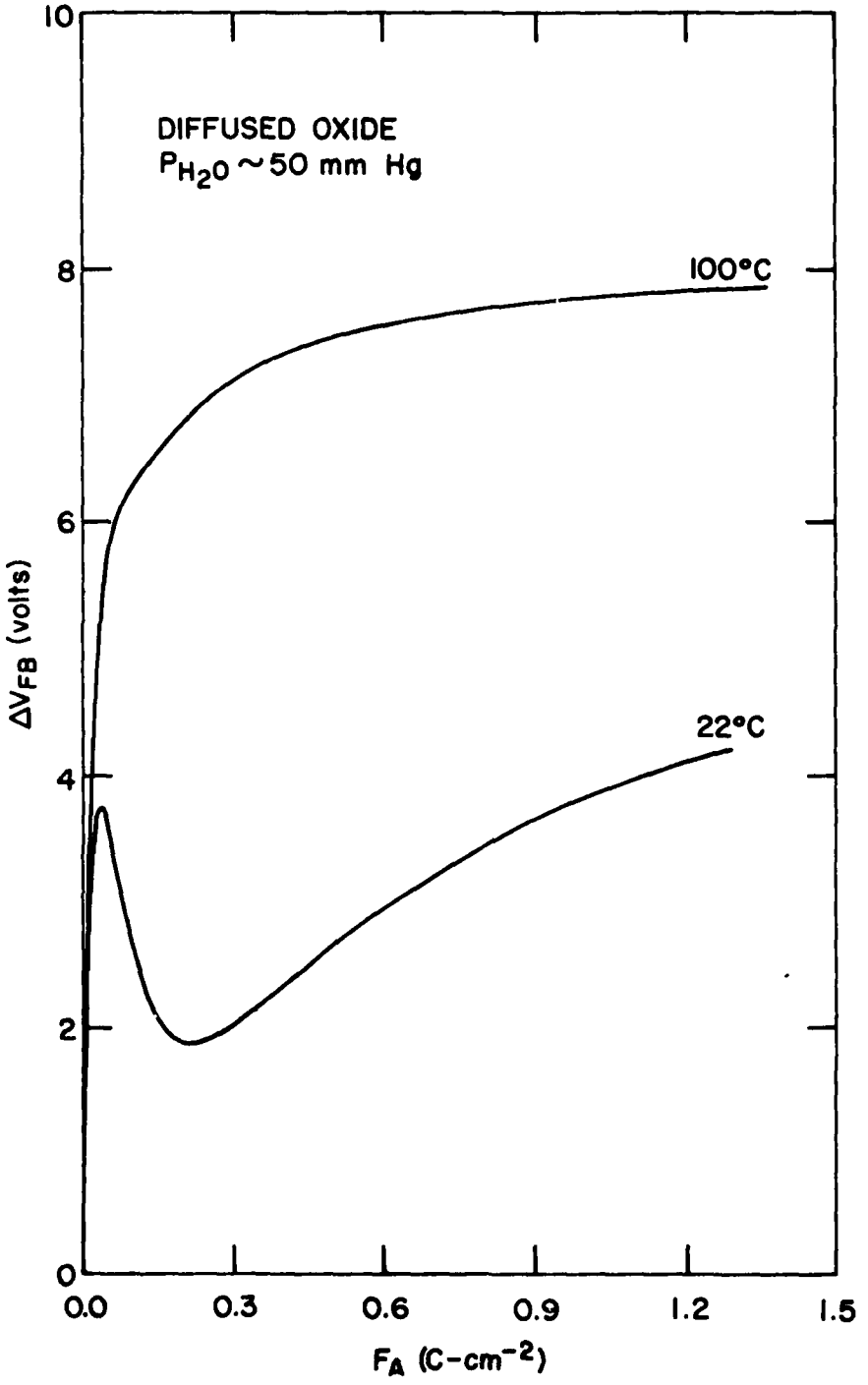

DIFFUSED OXIDE
$P_{H_2O} \sim 50$ mm Hg
100°C
22°C
ΔV_{FB} (volts)
F_A (C-cm^{-2})
0
2
4
6
8
10
0.0
0.3
0.6
0.9
1.2
1.5

FIGURE 3

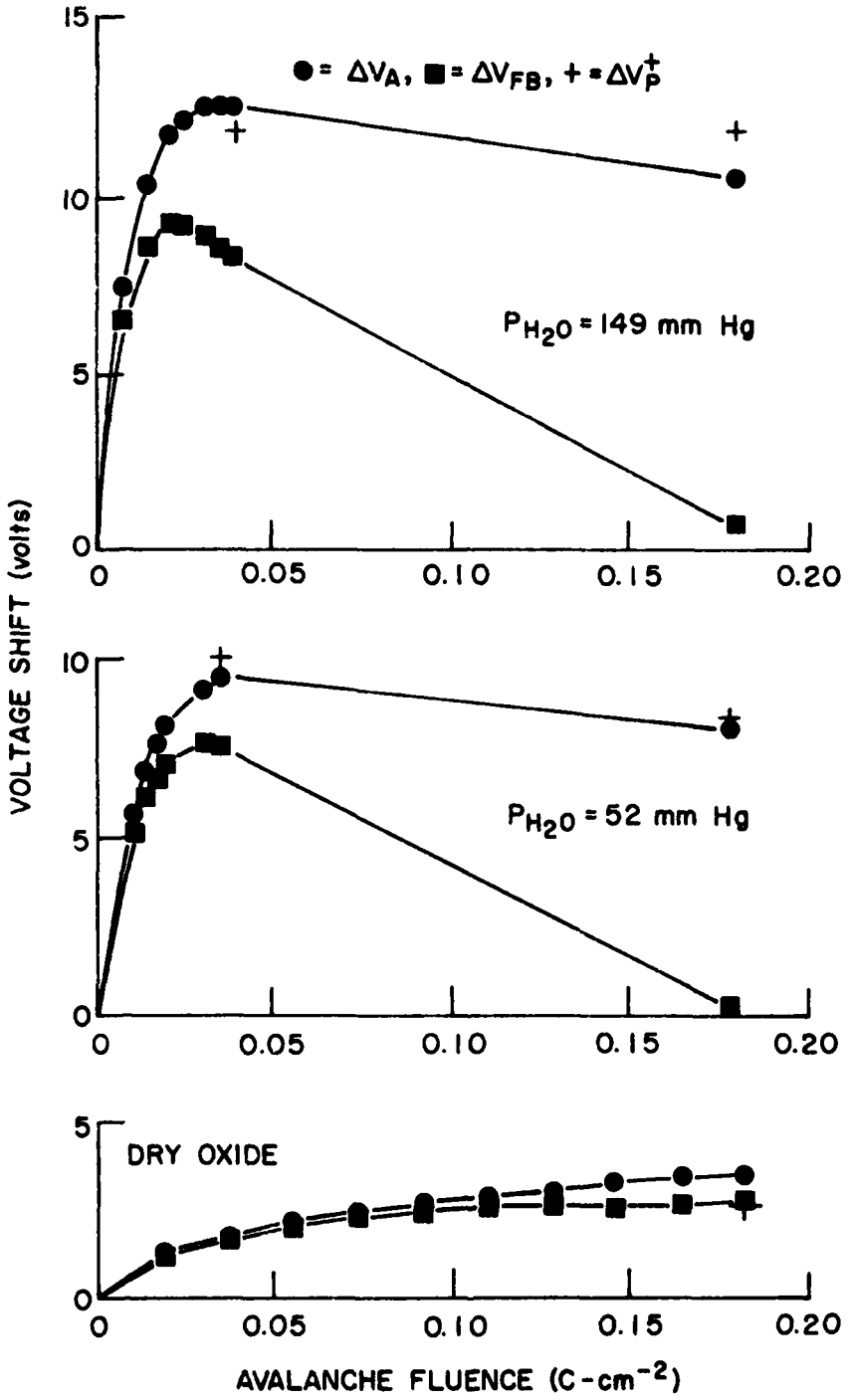

15
10
5
0
● = ΔV_A, ■ = ΔV_FB, + = ΔV_P^+
P_H2O = 149 mm Hg
0
0.05
0.10
0.15
0.20
10
5
0
P_H2O = 52 mm Hg
0
0.05
0.10
0.15
0.20
5
0
DRY OXIDE
0
0.05
0.10
0.15
0.20
VOLTAGE SHIFT (volts)
AVALANCHE FLUENCE (C-cm^-2)

FIGURE 4

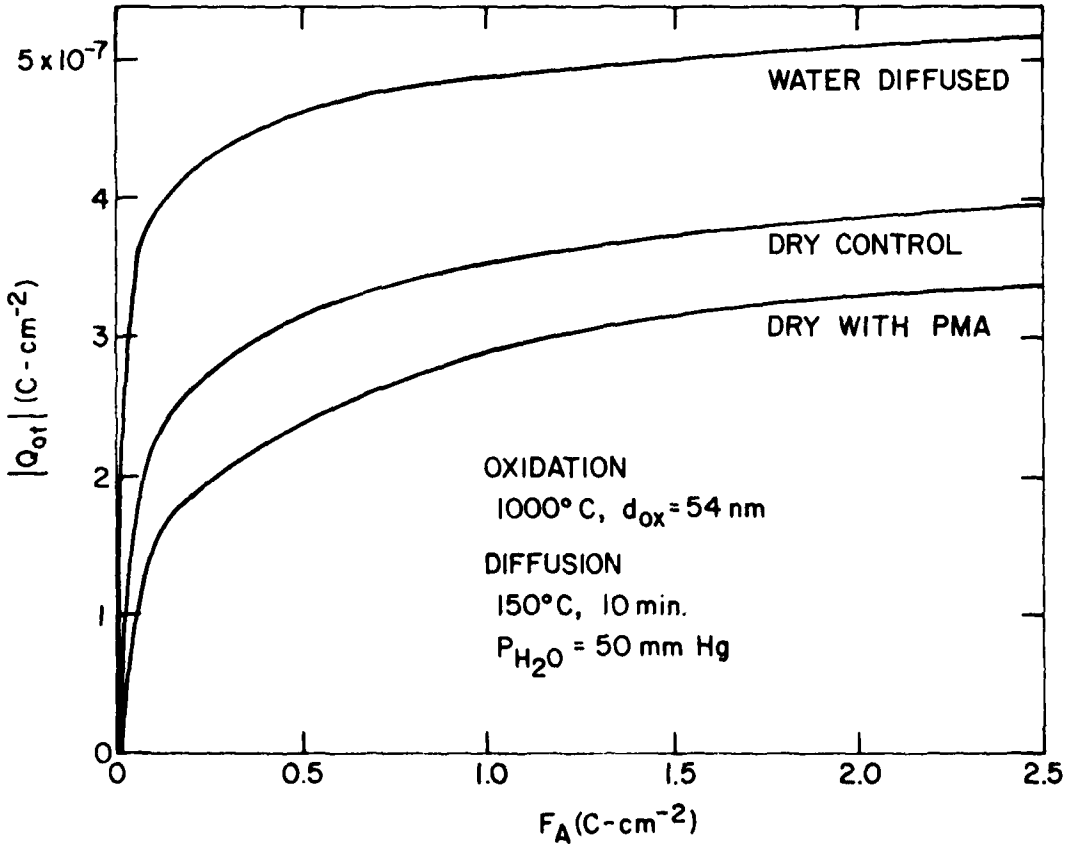

5 x 10⁻⁷
4
3
2
1
0
|Qot| (C-cm⁻²)
WATER DIFFUSED
DRY CONTROL
DRY WITH PMA
OXIDATION
1000° C, dox = 54 nm
DIFFUSION
150°C, 10 min.
PH2O = 50 mm Hg
0
0.5
1.0
1.5
2.0
2.5
FA(C-cm⁻²)

FIGURE 5

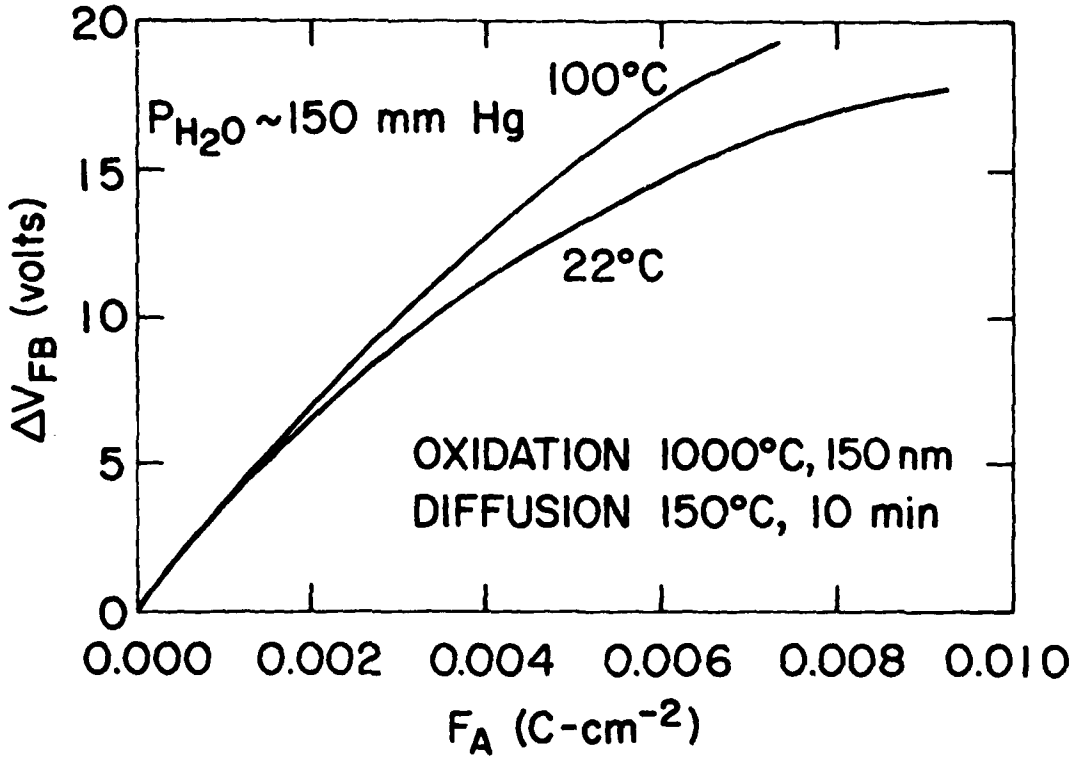

20
15
10
5
0
ΔV_{FB} (volts)
P_{H_2O} ~150 mm Hg
100°C
22°C
OXIDATION 1000°C, 150 nm
DIFFUSION 150°C, 10 min
0.000
0.002
0.004
0.006
0.008
0.010
F_A (C-cm^{-2})

FIGURE 6

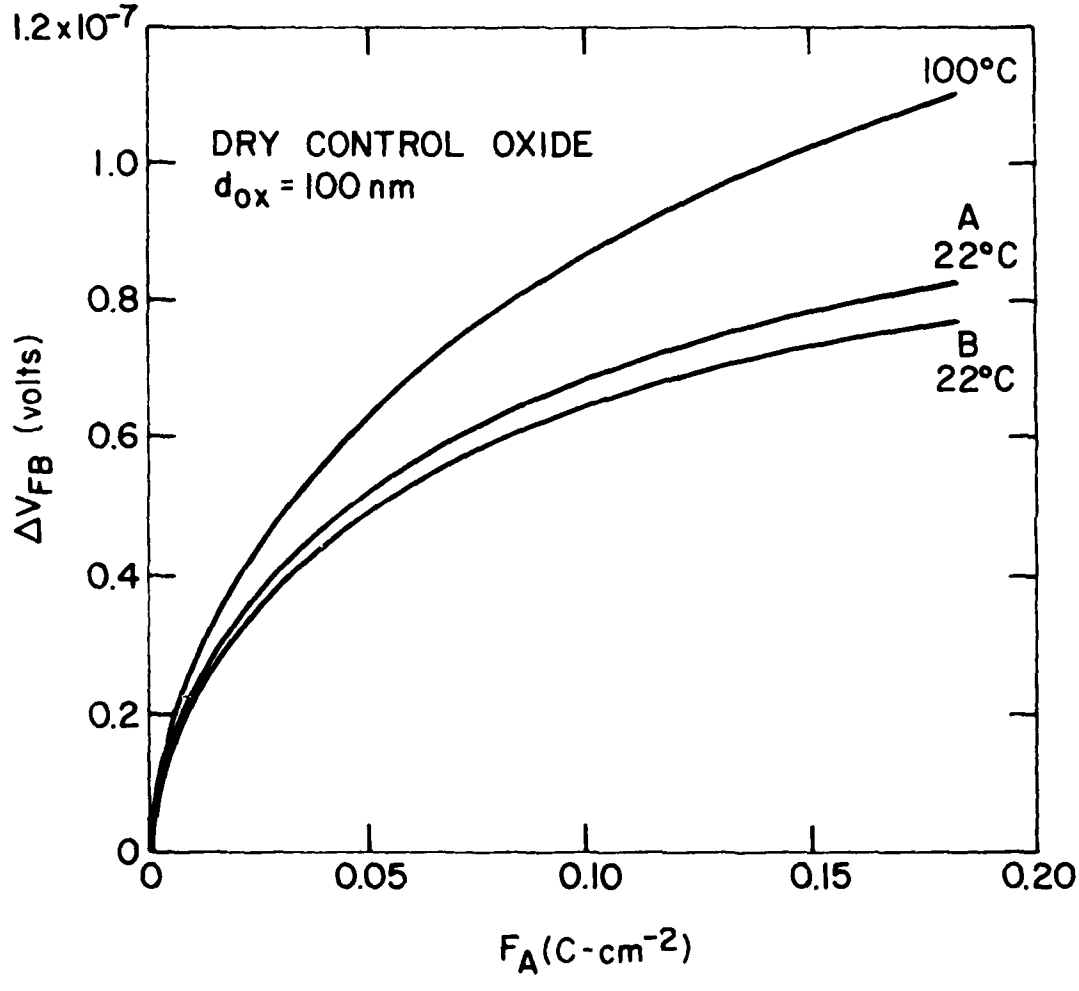

1.2x10⁻⁷
1.0
0.8
0.6
0.4
0.2
0
ΔV_FB (volts)
DRY CONTROL OXIDE
d_ox = 100 nm
100°C
A
22°C
B
22°C
0
0.05
0.10
0.15
0.20
F_A(C-cm⁻²)

FIGURE 7

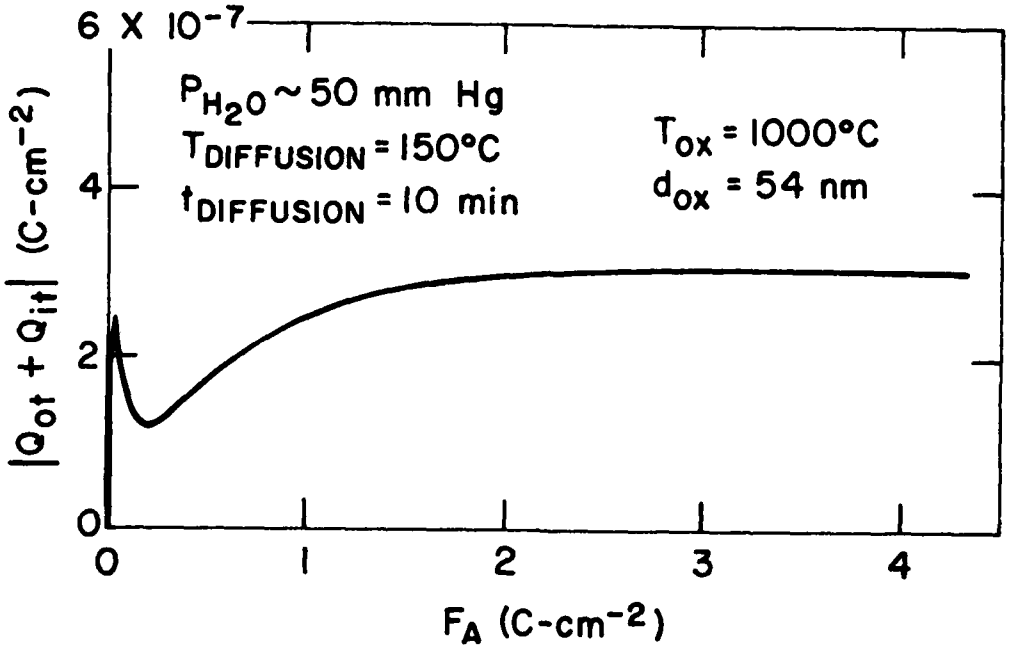

6 X 10⁻⁷
4
2
0
$P_{H_2O} \sim 50$ mm Hg
$T_{DIFFUSION} = 150°C$
$t_{DIFFUSION} = 10$ min
$T_{ox} = 1000°C$
$d_{ox} = 54$ nm
$|Q_{ot} + Q_{it}|$ (C-cm^{-2})
0
1
2
3
4
F_A (C-cm^{-2})

FIGURE 8

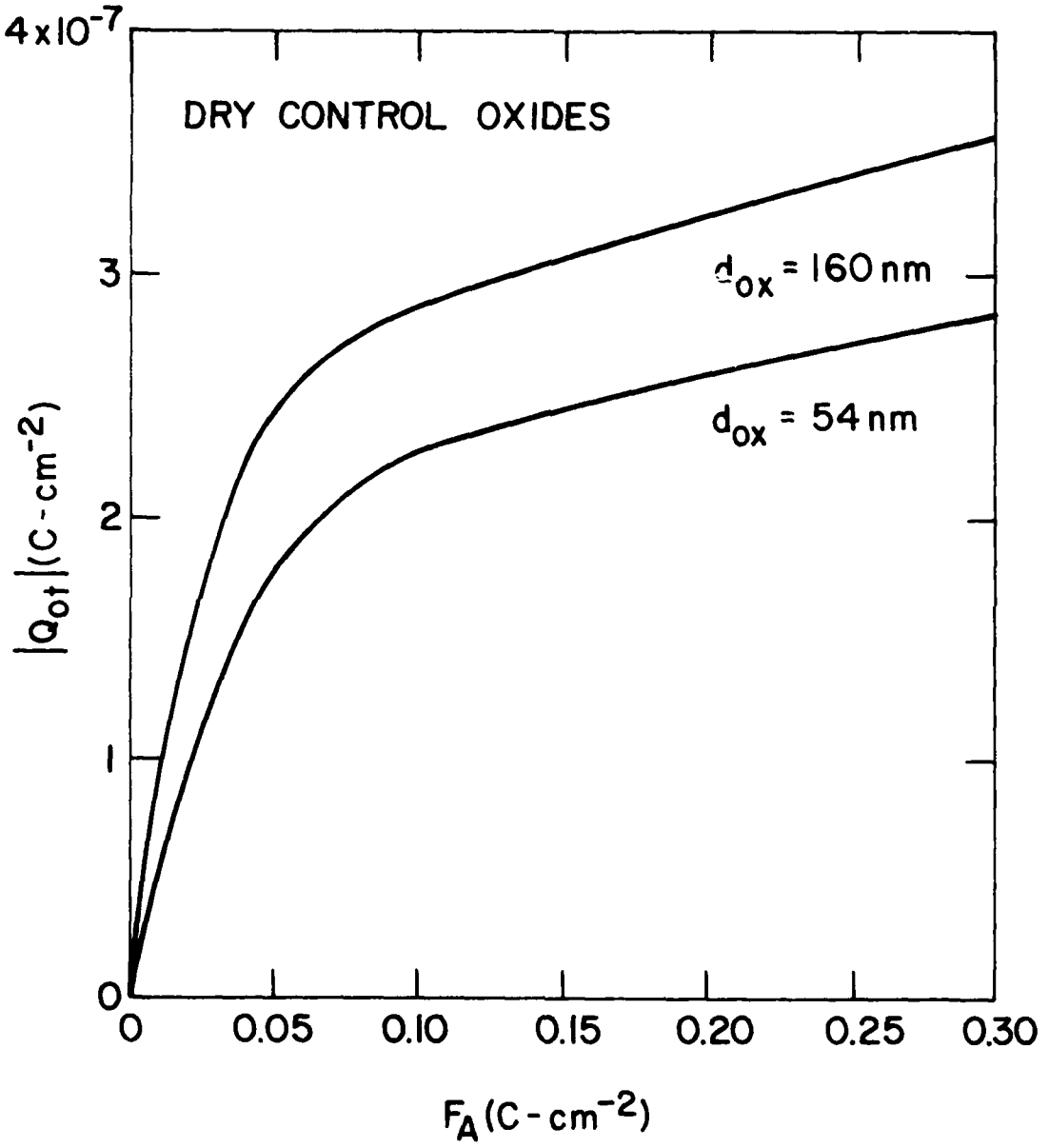

4x10⁻⁷
DRY CONTROL OXIDES
d_ox = 160 nm
d_ox = 54 nm
3
2
1
0
|Q_ot| (C-cm⁻²)
0
0.05
0.10
0.15
0.20
0.25
0.30
F_A (C-cm⁻²)

FIGURE 9

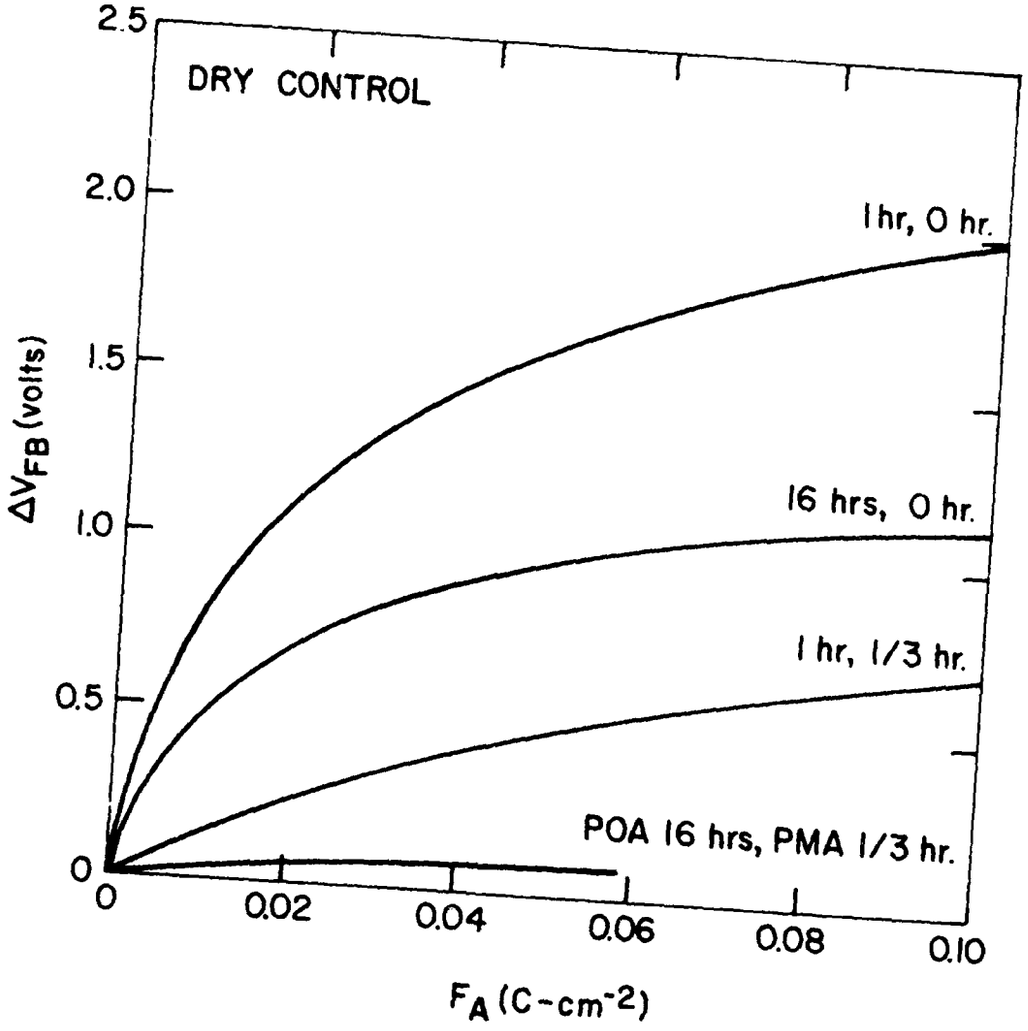

DRY CONTROL
1 hr, 0 hr.
16 hrs, 0 hr.
1 hr, 1/3 hr.
POA 16 hrs, PMA 1/3 hr.
2.5
2.0
1.5
1.0
0.5
0
0
0.02
0.04
0.06
0.08
0.10
ΔVFB (volts)
FA (C-cm-2)

FIGURE 10

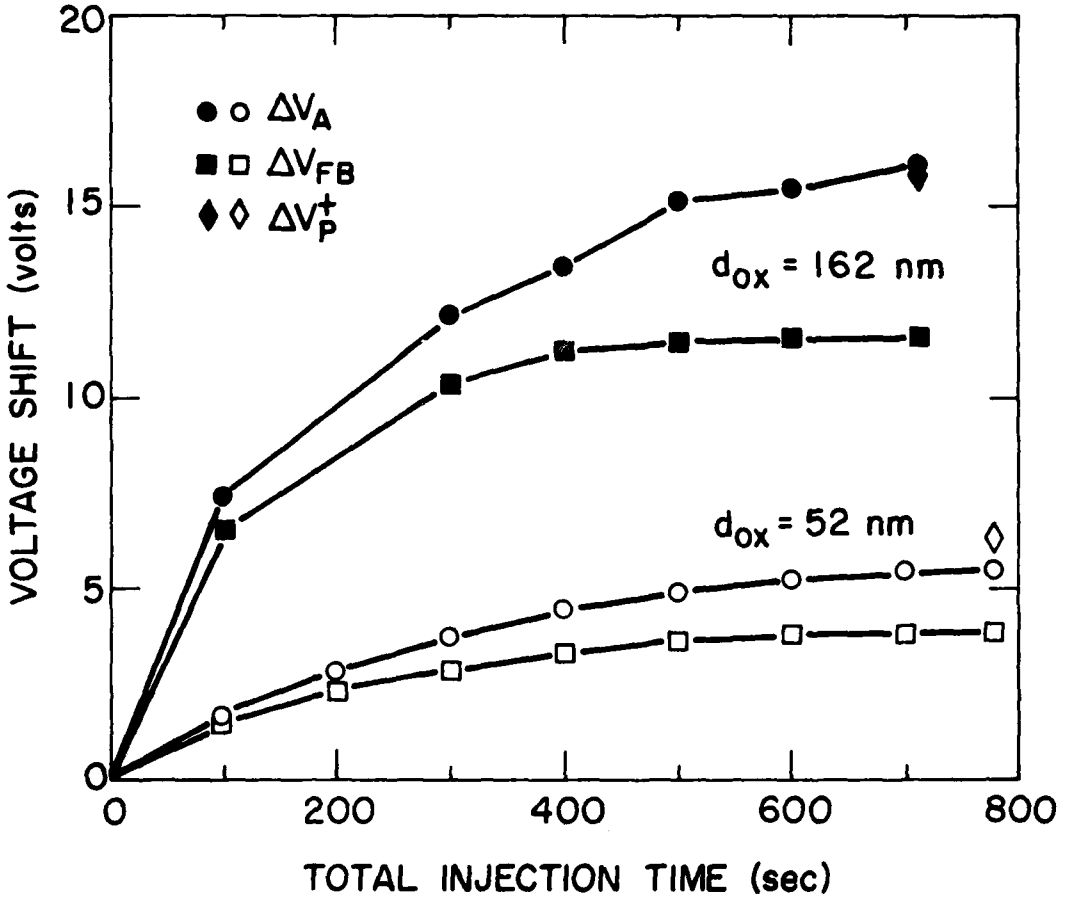

20
15
10
5
0
VOLTAGE SHIFT (volts)
● ○ ΔV_A
■ □ ΔV_FB
♦ ◊ ΔV_P^+
d_ox = 162 nm
d_ox = 52 nm
0
200
400
600
800
TOTAL INJECTION TIME (sec)

FIGURE 11

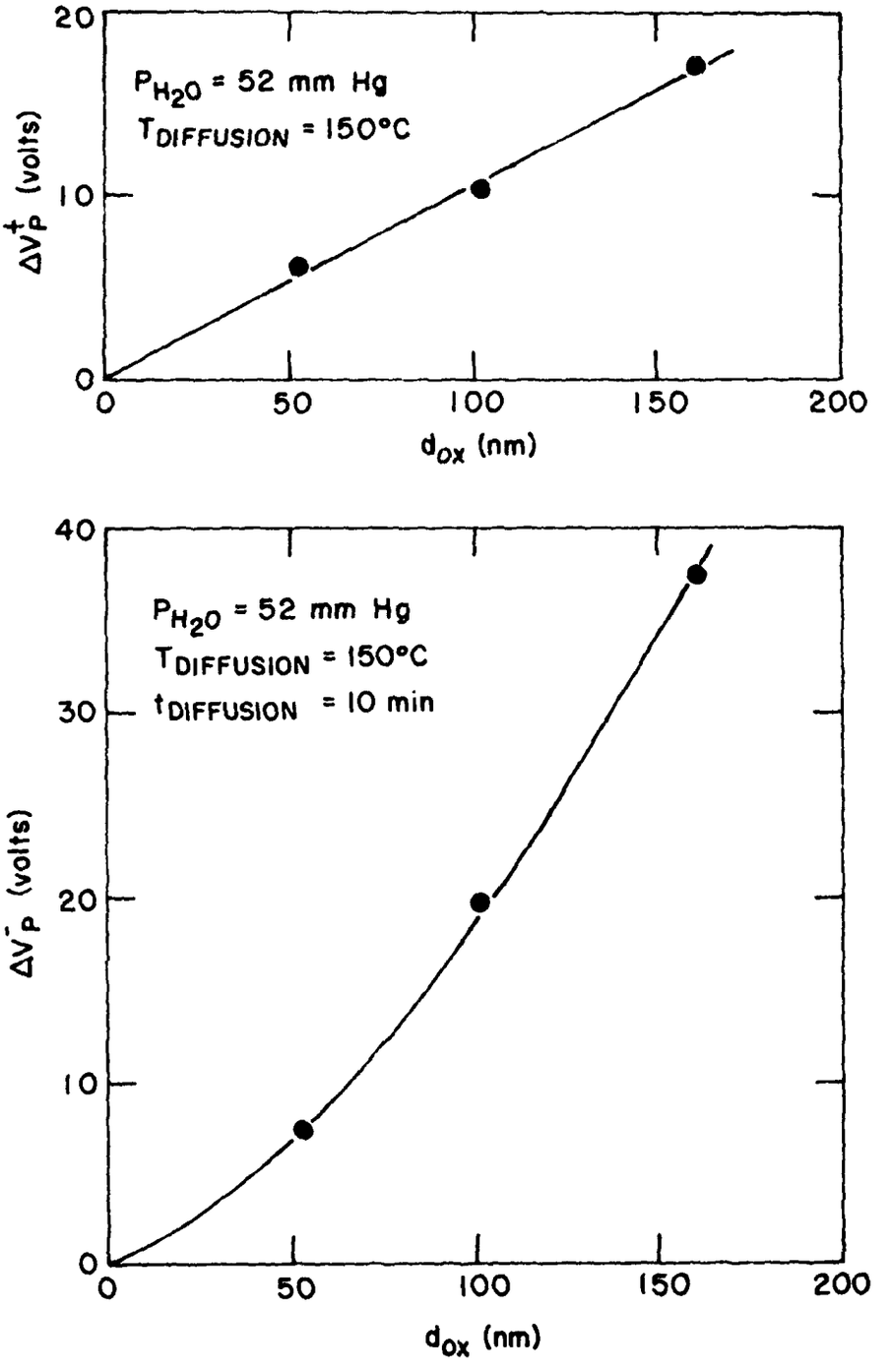
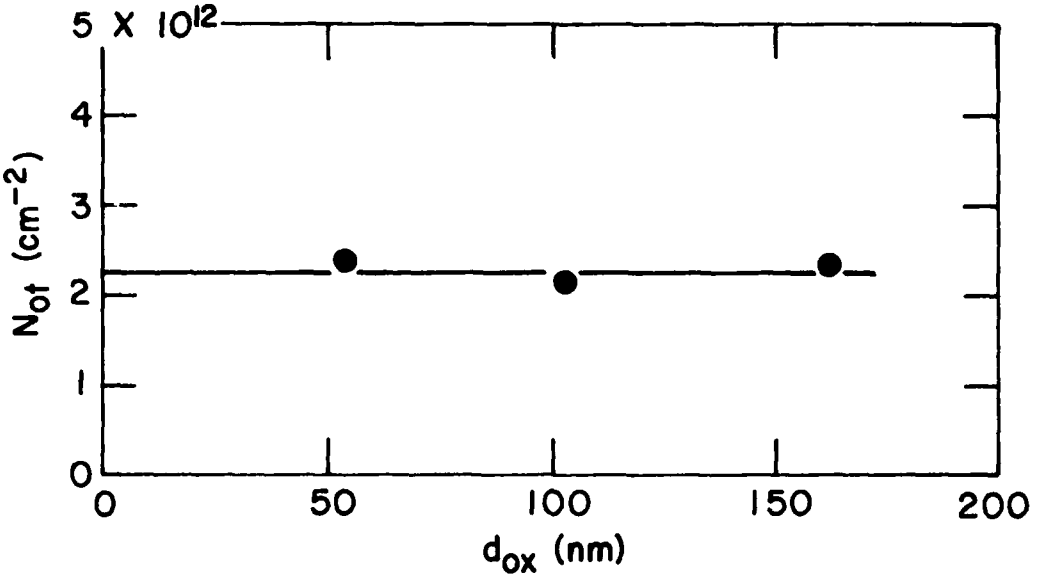

20
10
0
P_{H_2O} = 52 mm Hg
$T_{DIFFUSION}$ = 150°C
ΔV_P^+ (volts)
0
50
100
150
200
d_{ox} (nm)
40
30
20
10
0
P_{H_2O} = 52 mm Hg
$T_{DIFFUSION}$ = 150°C
$t_{DIFFUSION}$ = 10 min
ΔV_P^- (volts)
0
50
100
150
200
d_{ox} (nm)

FIGURE 12



P_{H_2O} = 52 mm Hg, $T_{DIFFUSION}$ = 150°C, 10 min

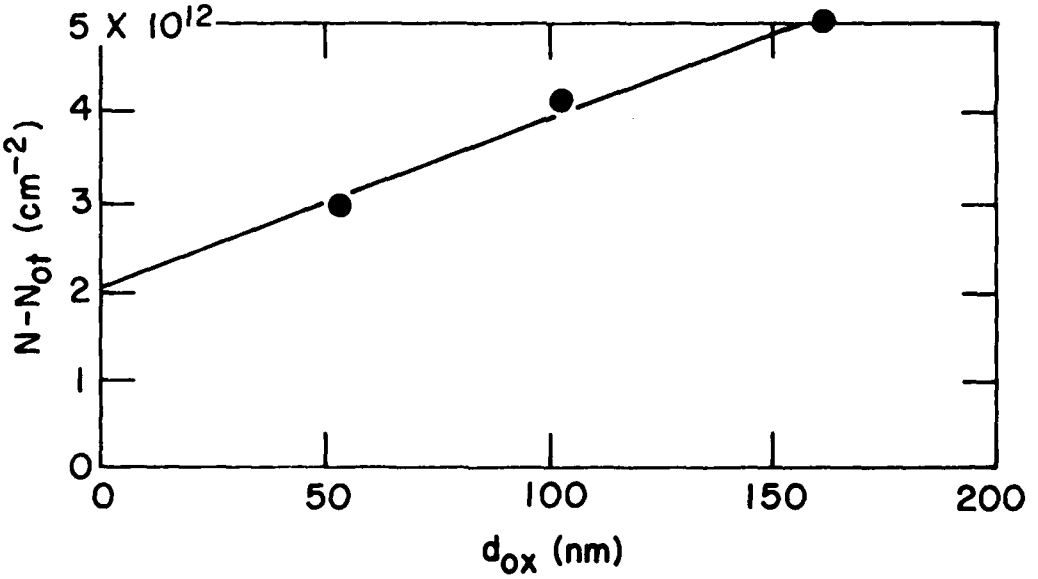


FIGURE 13

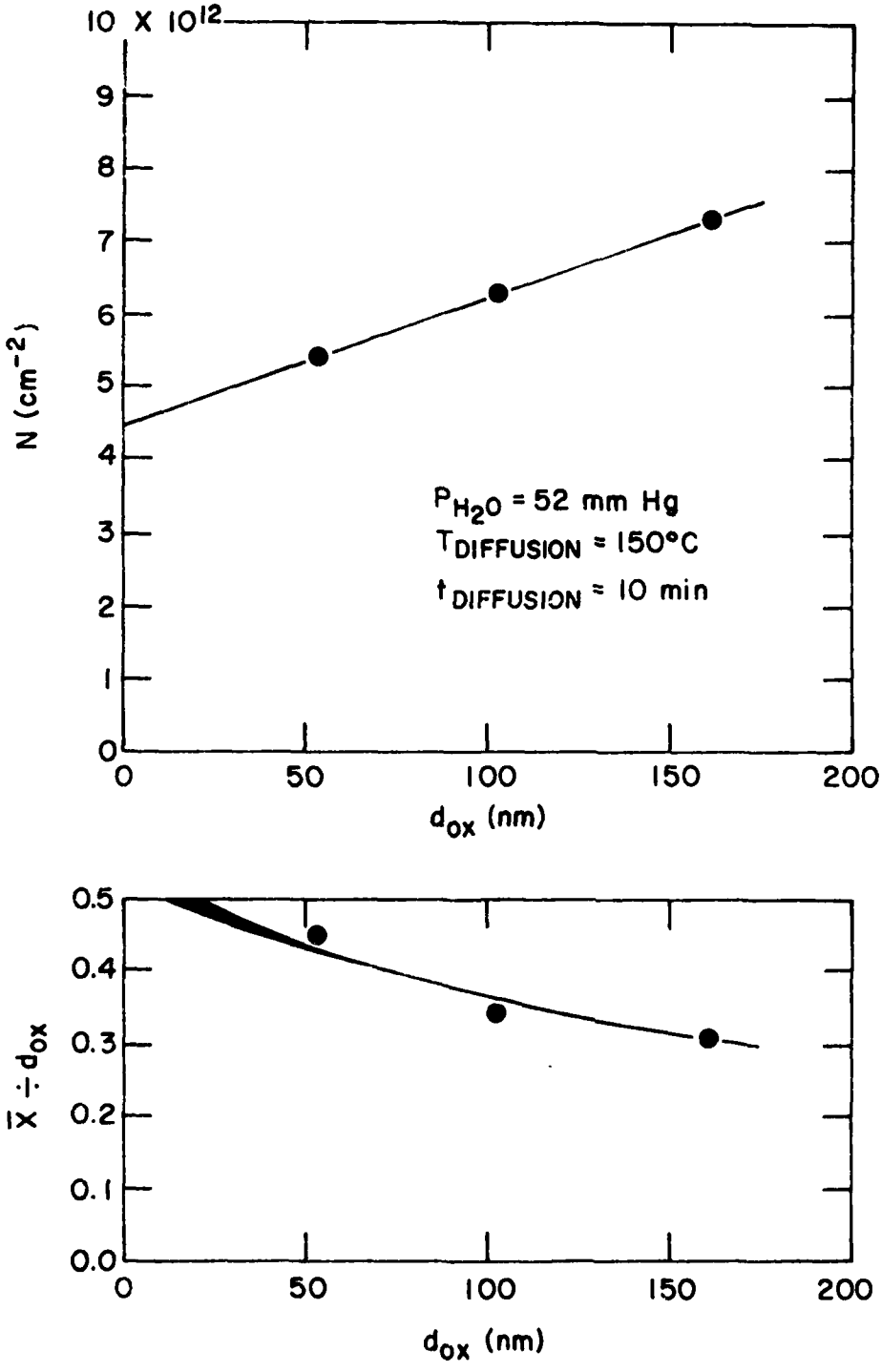

10 X 10^12
9
8
7
6
5
4
3
2
1
0
N (cm^-2)
P_H2O = 52 mm Hg
T_DIFFUSION = 150°C
t_DIFFUSION = 10 min
0
50
100
150
200
d_ox (nm)
0.5
0.4
0.3
0.2
0.1
0.0
X̄ ÷ d_ox
0
50
100
150
200
d_ox (nm)

FIGURE 14

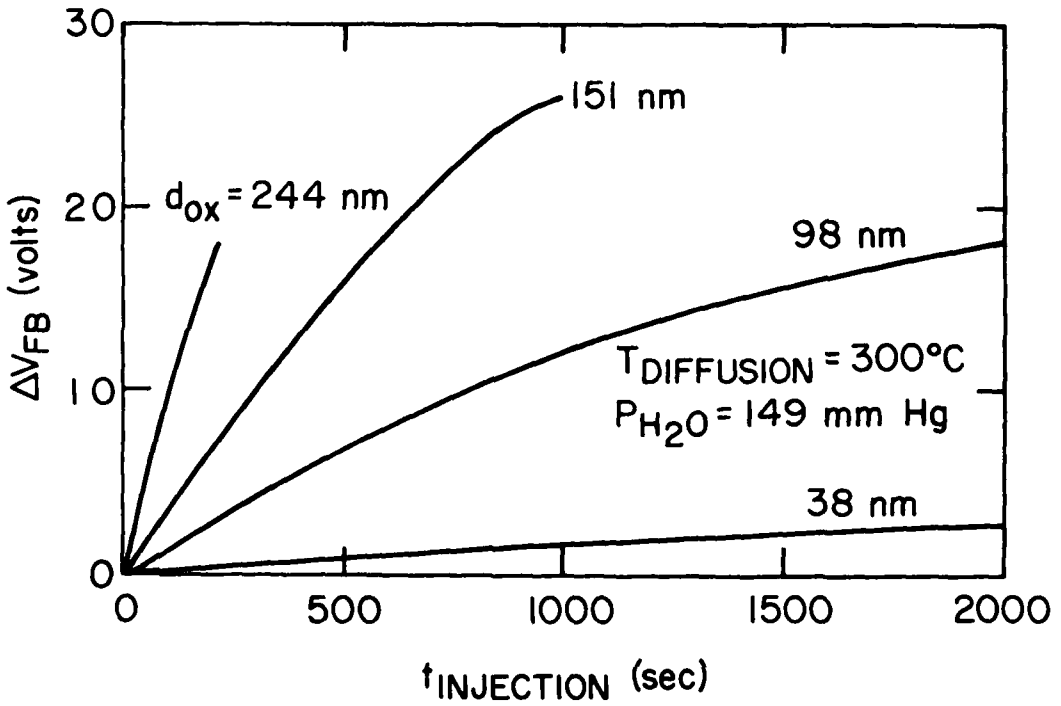

30
20
10
0
ΔV_{FB} (volts)
d_{ox} = 244 nm
151 nm
98 nm
38 nm
$T_{DIFFUSION}$ = 300°C
P_{H_2O} = 149 mm Hg
0
500
1000
1500
2000
$t_{INJECTION}$ (sec)

FIGURE 15

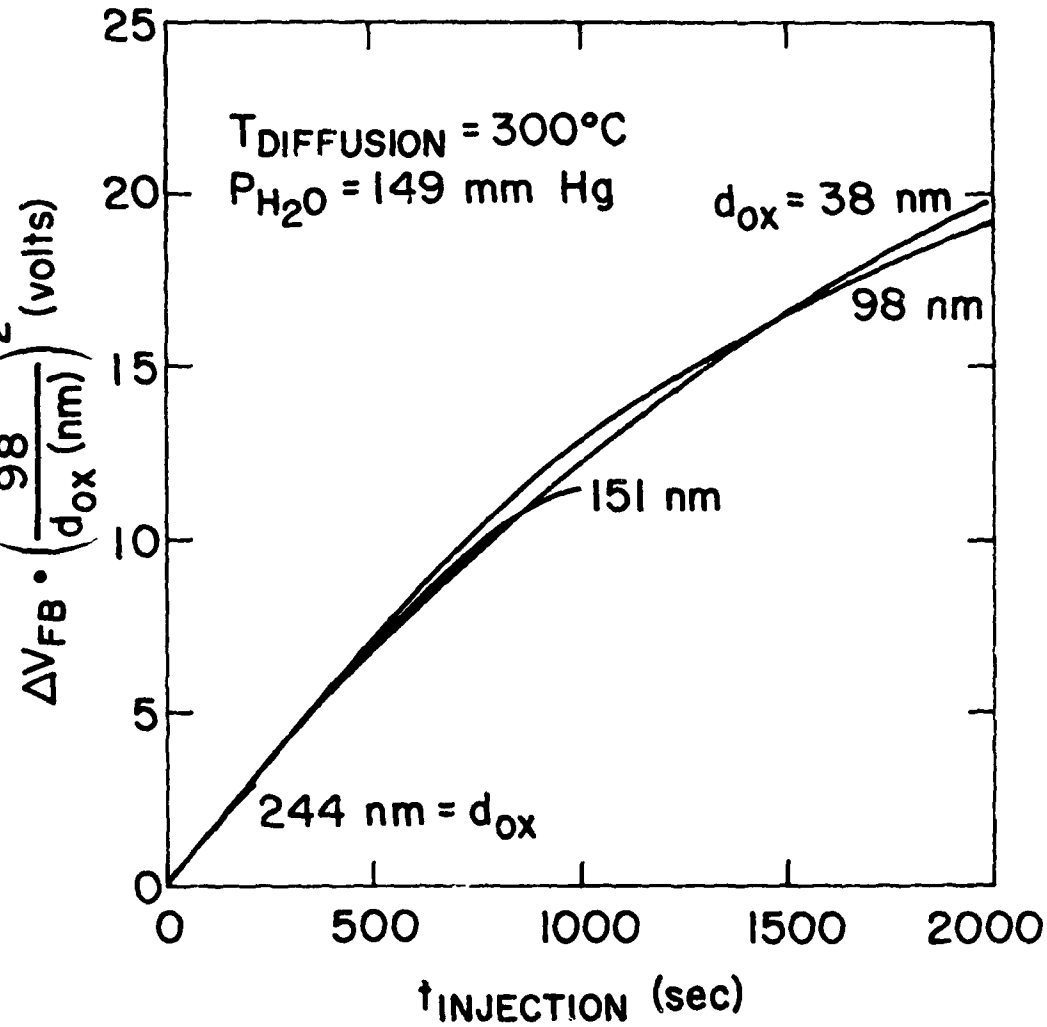

25
20
15
10
5
0
0
500
1000
1500
2000
$T_{DIFFUSION}$ = 300°C
P_{H_2O} = 149 mm Hg
d_{ox} = 38 nm
98 nm
151 nm
244 nm = d_{ox}
$\Delta V_{FB} \cdot \left(\frac{98}{d_{ox}\,(nm)}\right)^2$ (volts)
$t_{INJECTION}$ (sec)

FIGURE 16

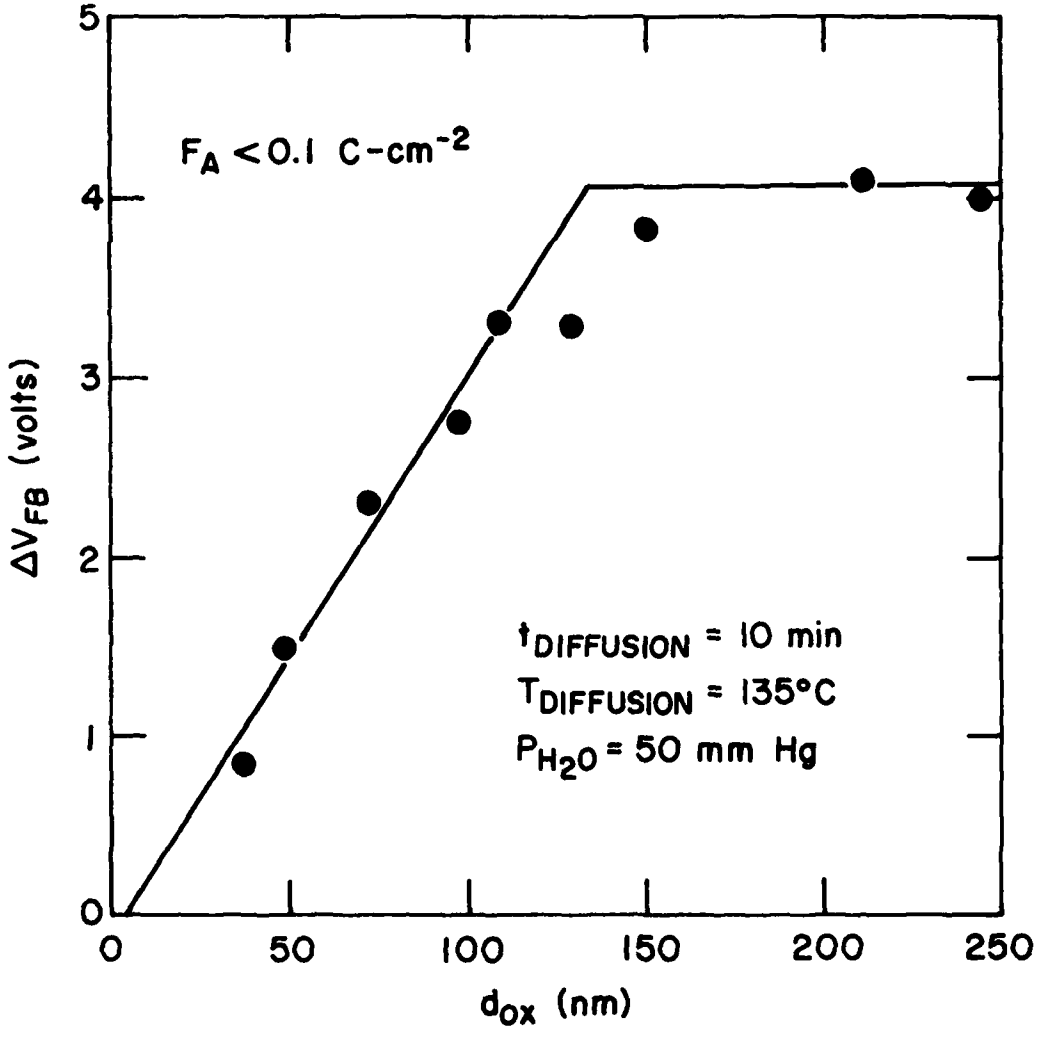

5
4
3
2
1
0
ΔV_{FB} (volts)
$F_A < 0.1$ C-cm^{-2}
$t_{DIFFUSION}$ = 10 min
$T_{DIFFUSION}$ = 135°C
P_{H_2O} = 50 mm Hg
0
50
100
150
200
250
d_{ox} (nm)

FIGURE 17

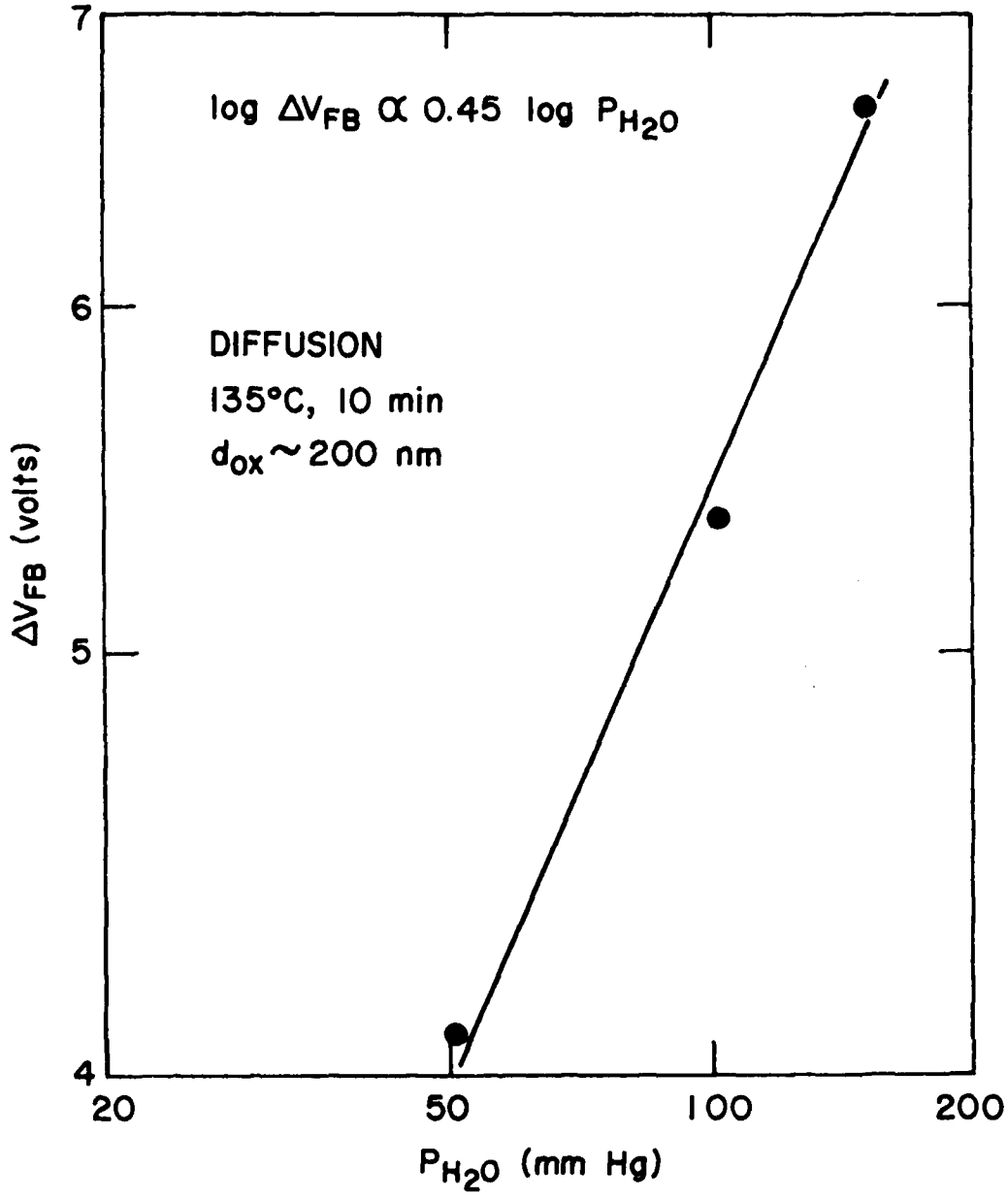

log $\Delta V_{FB} \propto 0.45$ log P_{H_2O}
DIFFUSION
135°C, 10 min
$d_{ox} \sim 200$ nm
ΔV_{FB} (volts)
7
6
5
4
20
50
100
200
P_{H_2O} (mm Hg)

FIGURE 18

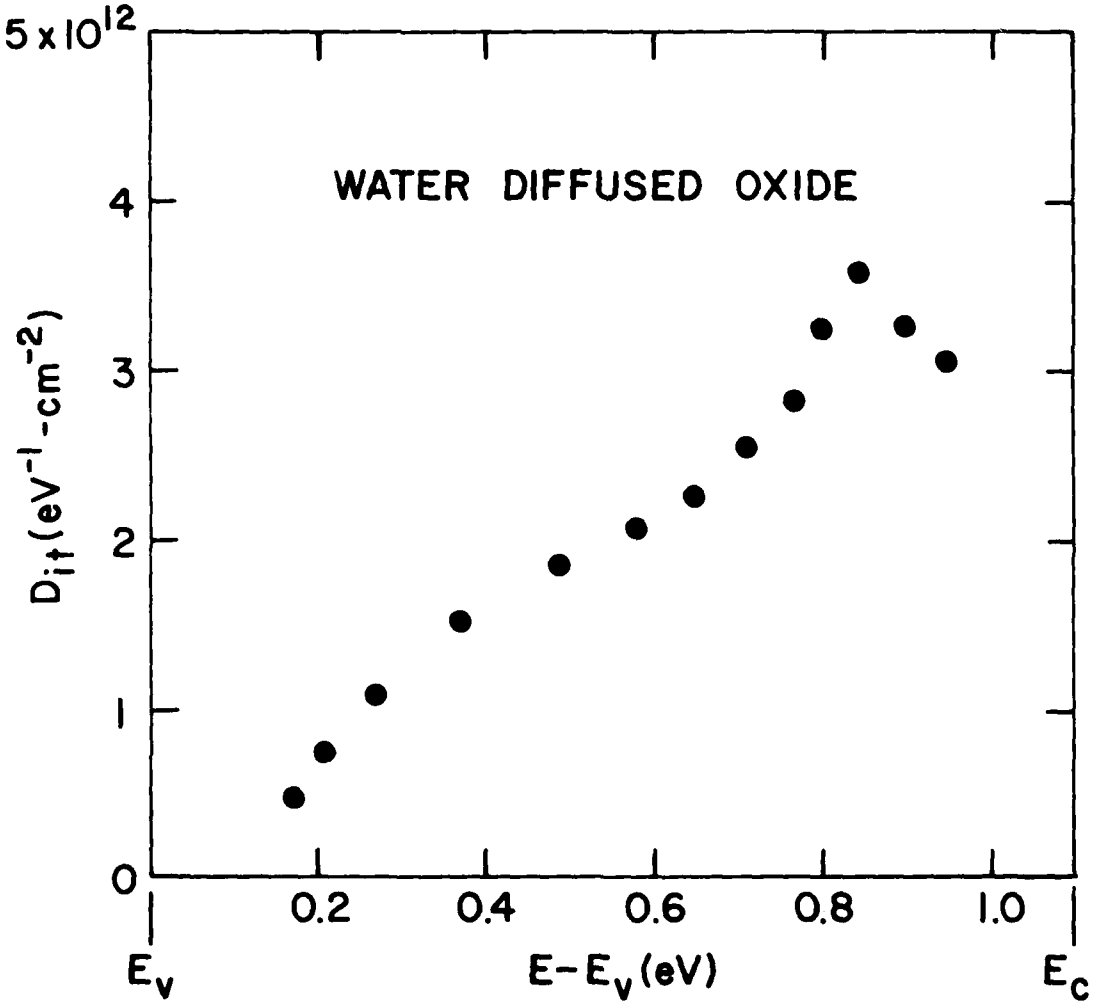

5 x 10^12
4
3
2
1
0
WATER DIFFUSED OXIDE
D_it (eV^-1 - cm^-2)
0.2
0.4
0.6
0.8
1.0
E_V
E - E_V (eV)
E_C

FIGURE 19

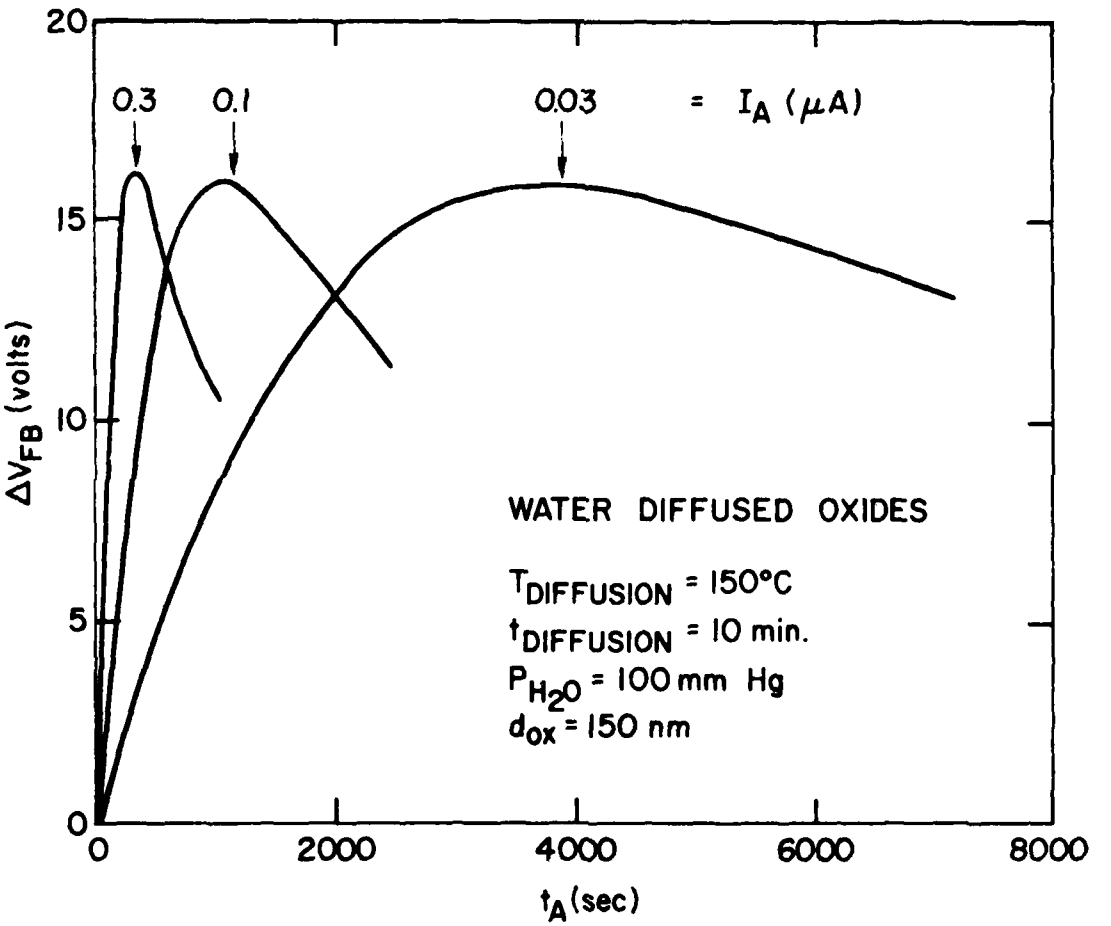

20
15
10
5
0
0.3
0.1
0.03
= I_A (μA)
ΔV_{FB} (volts)
WATER DIFFUSED OXIDES
$T_{DIFFUSION}$ = 150°C
$t_{DIFFUSION}$ = 10 min.
P_{H_2O} = 100 mm Hg
d_{ox} = 150 nm
0
2000
4000
6000
8000
t_A(sec)

FIGURE 20

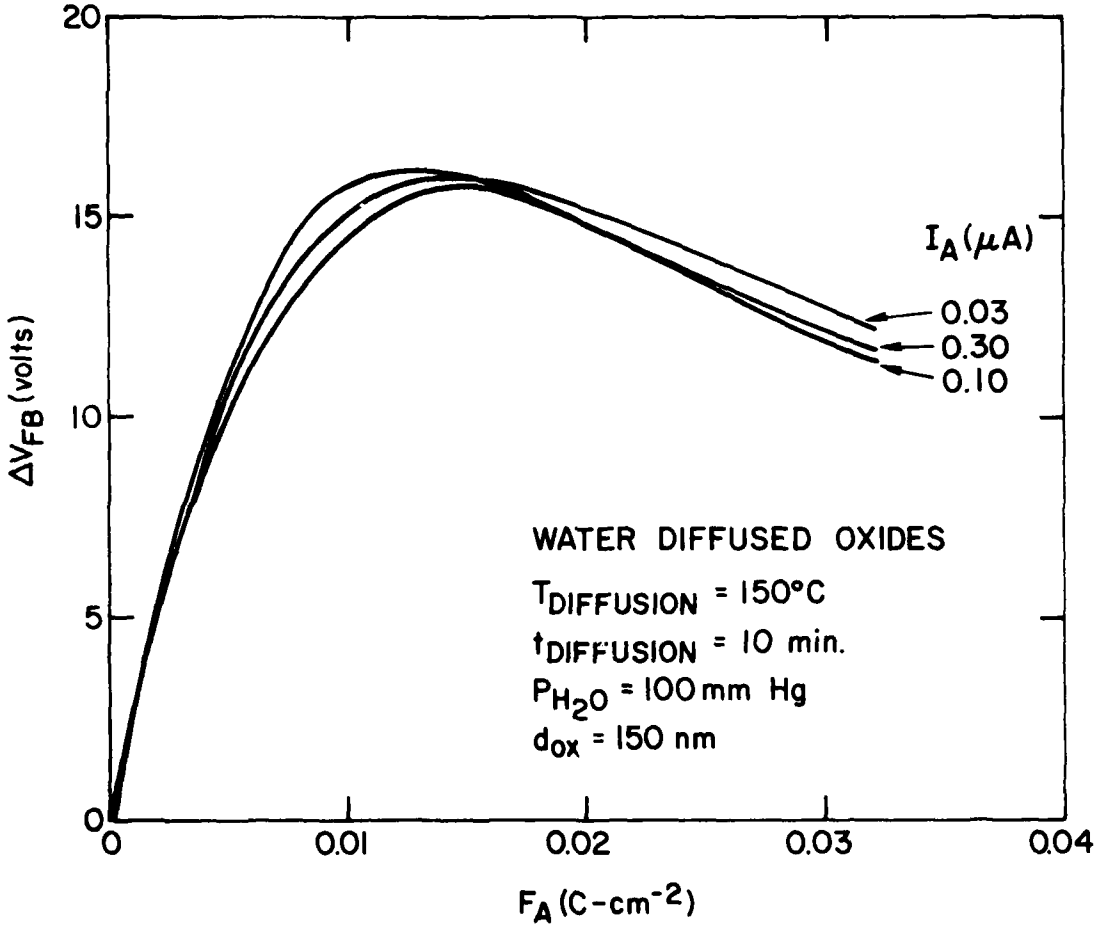

20
15
10
5
0
0
0.01
0.02
0.03
0.04
ΔV_{FB} (volts)
F_A (C-cm^{-2})
I_A (μA)
0.03
0.30
0.10
WATER DIFFUSED OXIDES
$T_{DIFFUSION}$ = 150°C
$t_{DIFFUSION}$ = 10 min.
P_{H_2O} = 100 mm Hg
d_{ox} = 150 nm

FIGURE 21

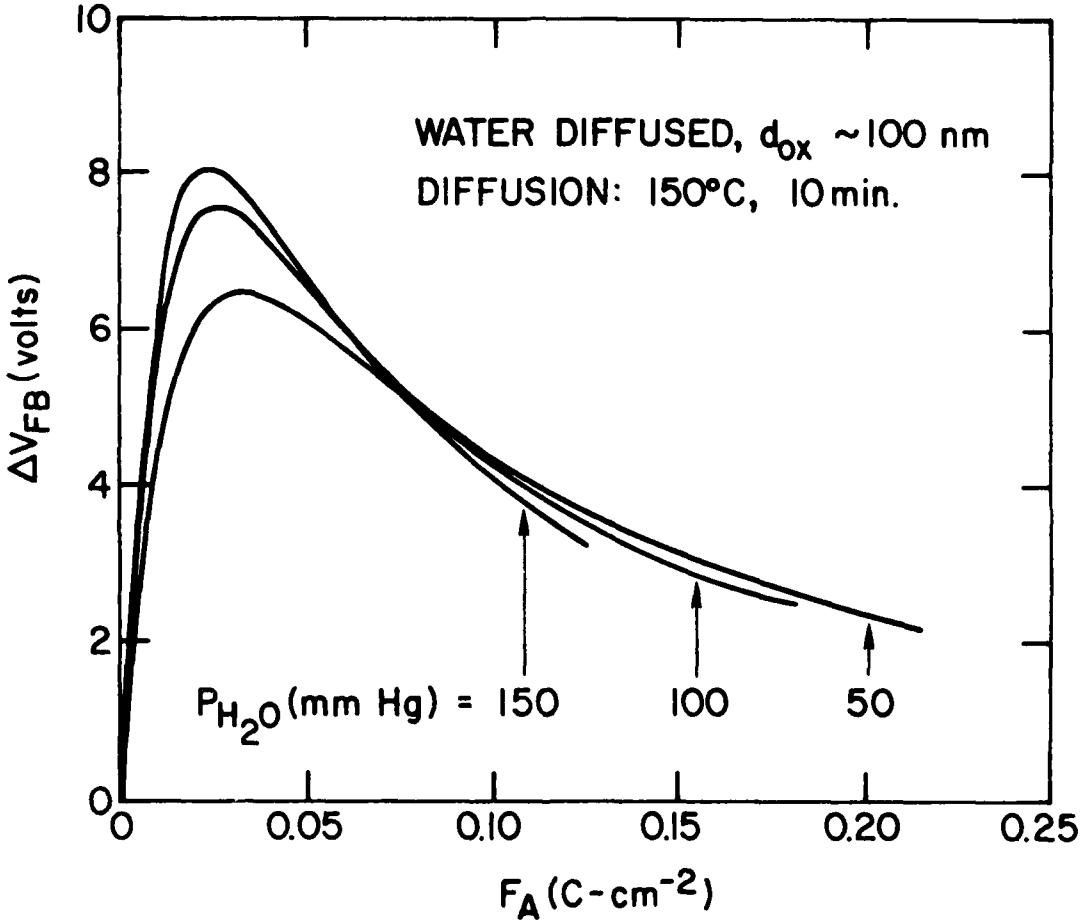

WATER DIFFUSED, d_{ox} ~100 nm
DIFFUSION: 150°C, 10 min.
P_{H_2O} (mm Hg) = 150
100
50
ΔV_{FB} (volts)
F_A (C-cm^{-2})
0
2
4
6
8
10
0
0.05
0.10
0.15
0.20
0.25

FIGURE 22

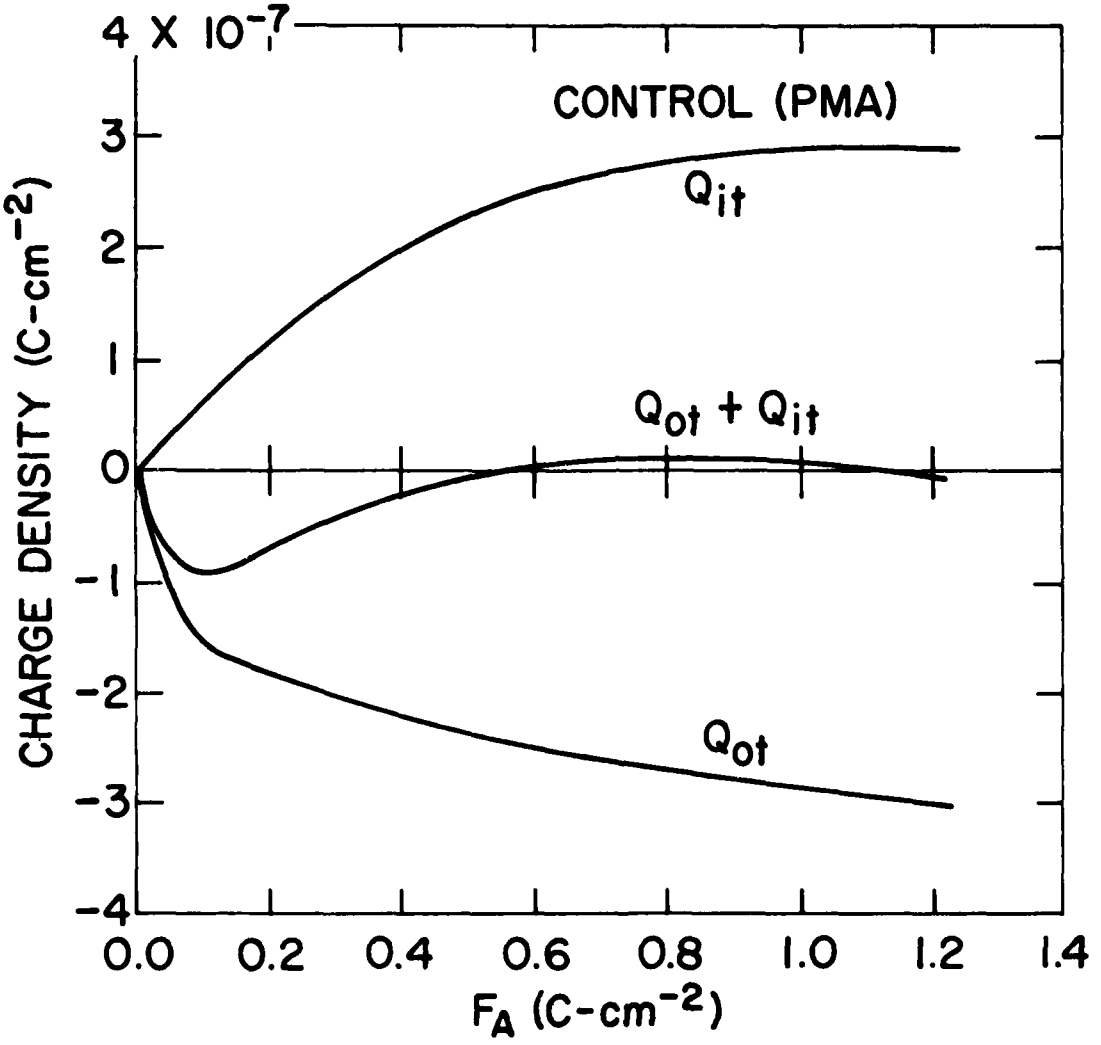

4 X 10⁻⁷
CONTROL (PMA)
Qit
Qot + Qit
Qot
CHARGE DENSITY (C-cm⁻²)
3
2
1
0
-1
-2
-3
-4
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
FA (C-cm⁻²)

FIGURE 23

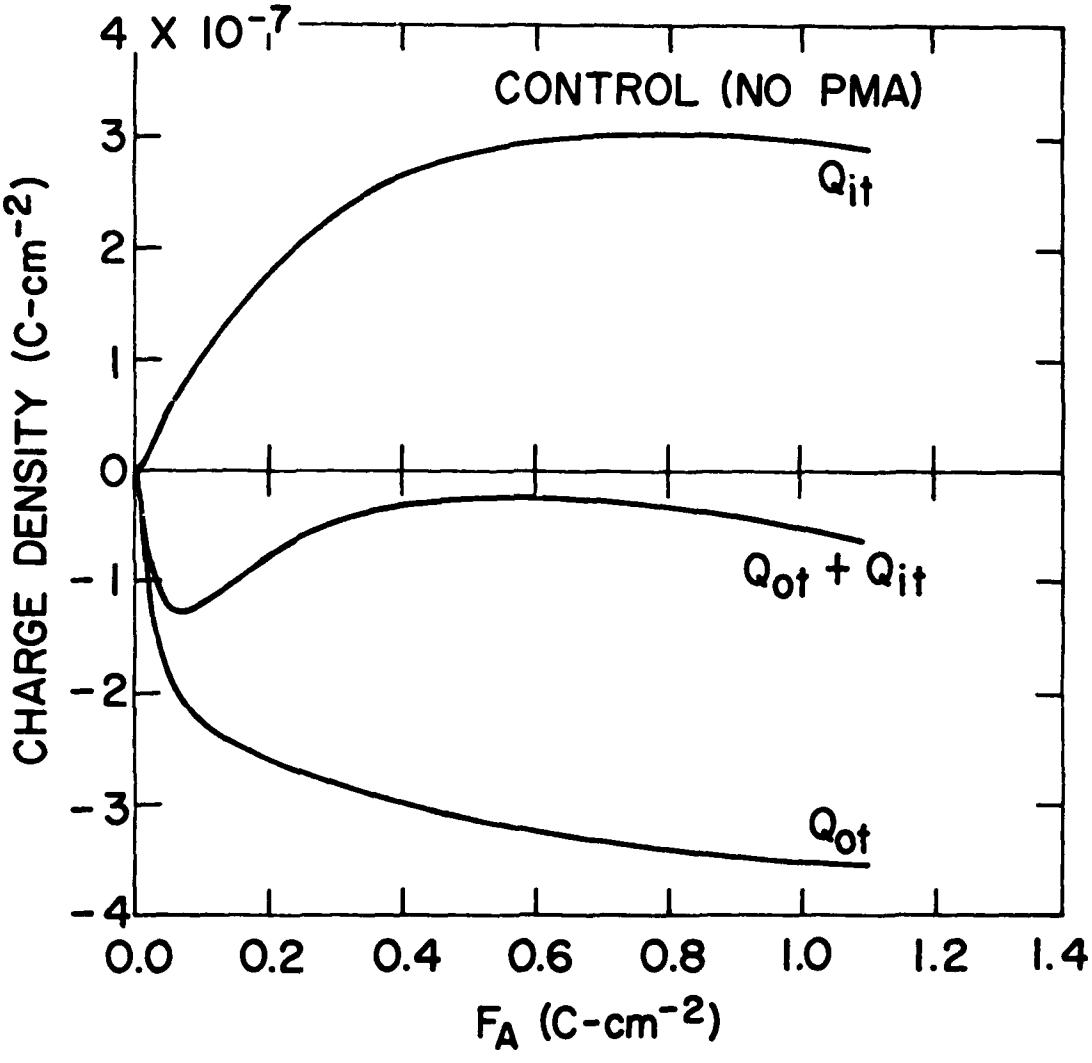

4 X 10⁻⁷
CONTROL (NO PMA)
3
2
1
0
-1
-2
-3
-4
CHARGE DENSITY (C-cm⁻²)
Qit
Qot + Qit
Qot
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
FA (C-cm⁻²)

FIGURE 24

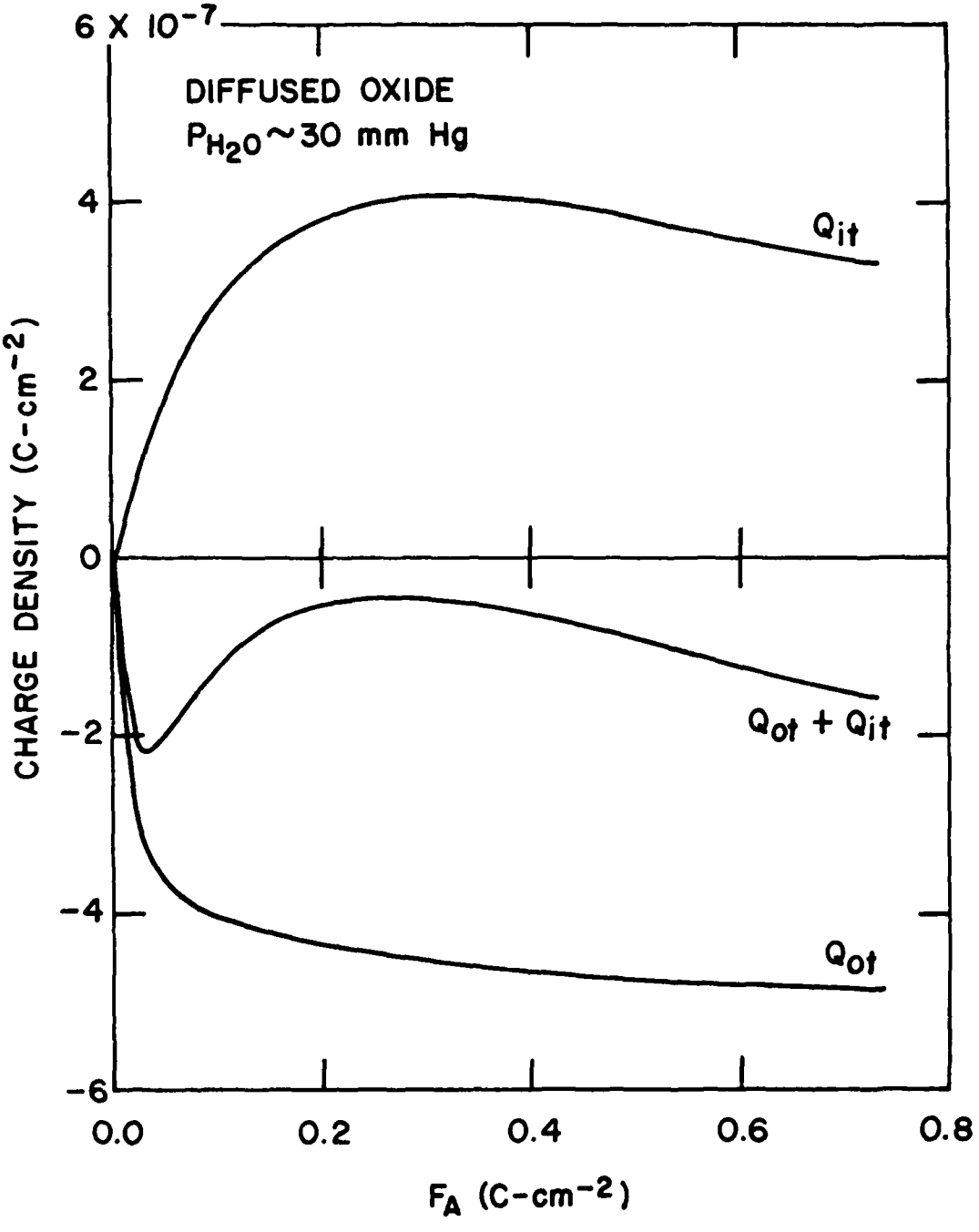

6 X 10⁻⁷
DIFFUSED OXIDE
P_H2O ~ 30 mm Hg
4
2
0
-2
-4
-6
Q_it
Q_ot + Q_it
Q_ot
CHARGE DENSITY (C-cm⁻²)
0.0
0.2
0.4
0.6
0.8
F_A (C-cm⁻²)

FIGURE 25

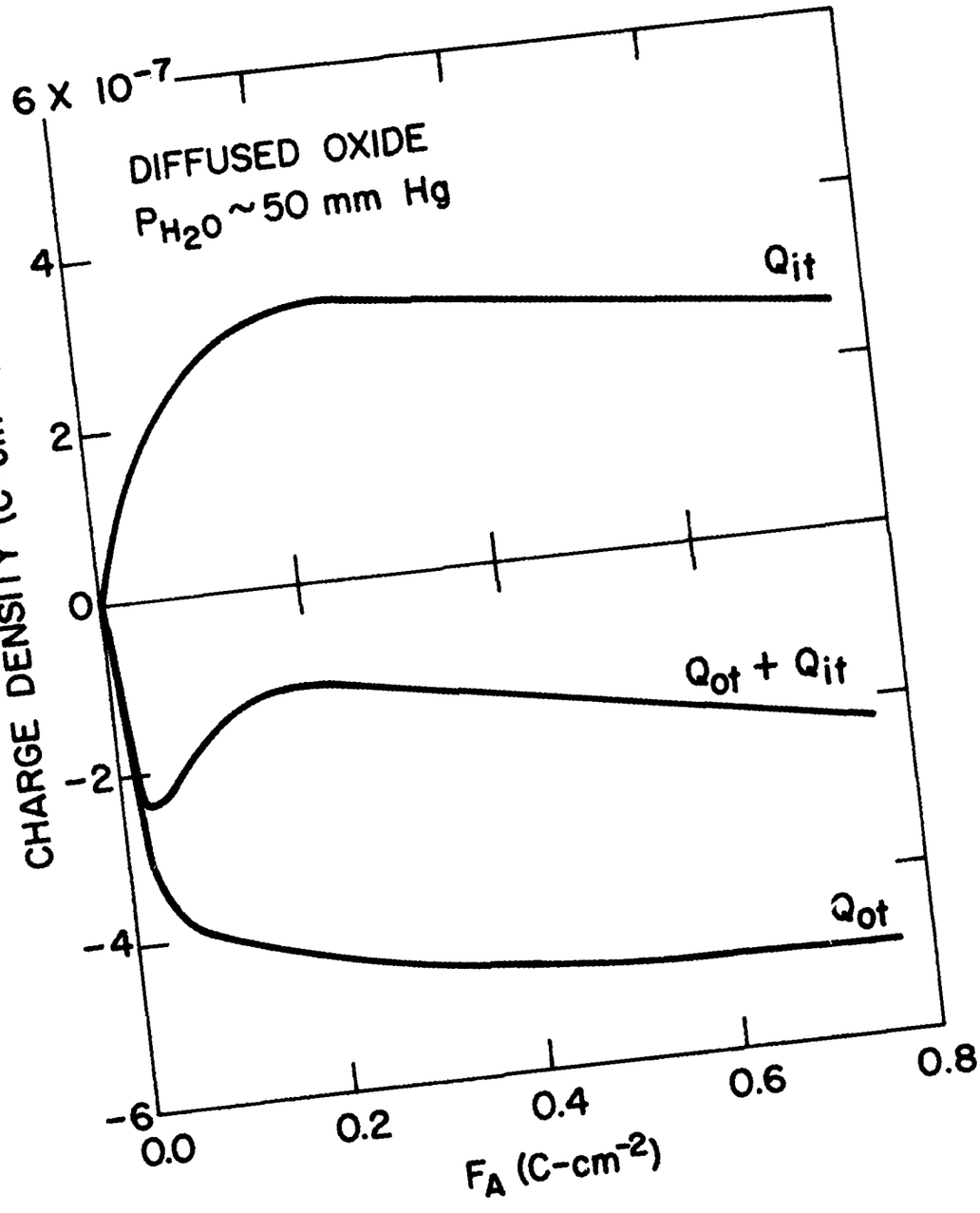

6 X 10⁻⁷
DIFFUSED OXIDE
P_H2O ~ 50 mm Hg
Qit
Qot + Qit
Qot
4
2
0
-2
-4
-6
0.0
0.2
0.4
0.6
0.8
CHARGE DENSITY (C-cm⁻²)
F_A (C-cm⁻²)

FIGURE 26

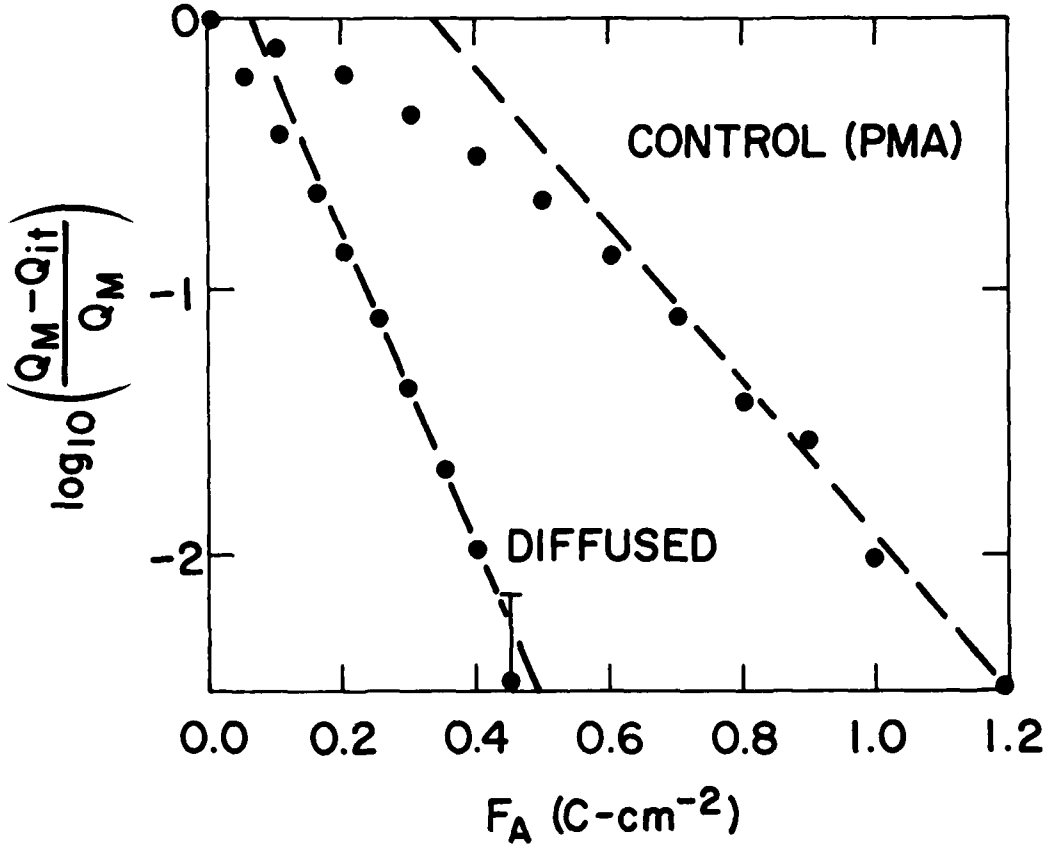

0
-1
-2
CONTROL (PMA)
DIFFUSED
$\log_{10}\left(\frac{Q_M - Q_{it}}{Q_M}\right)$
0.0
0.2
0.4
0.6
0.8
1.0
1.2
F_A (C-cm^{-2})

FIGURE 27

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